APPLICATION NOTE

AN-122

Breakdown Voltage Tests Including Bipolar Transistors

Overview

When first conceived, the tests now labeled as breakdown tests were single point, voltage-current tests. Some stepped voltage to reach a current, and some forced the current and measured voltage. When the tests were re-labeled as breakdown types, they were not changed to have attributes of breakdown tests found in the fast WLR Jramp and Vramp tests.

A couple of years ago, a major customer had problems making breakdown measurements within CMOS technologies. On-site applications assistance provided critical information that led to Reedholm making considerable changes in the RDS DOS 8.11 and RDS Intranet 1.30 software release.

In late 2009, a visit to a company running bipolar silicon processes provided direct evidence of bipolar transistor breakdown that led to more changes released in RDS DOS 8.12 and Intranet 1.31. In addition, instrumentation hardware changes were made to mitigate the effects of bipolar transistor breakdowns.

Customers running software older than RDS DOS 8.12 or Intranet 1.31 do not have all the enhancements described in this document. Patches are not available for earlier versions.

As can be seen from the RIresults array descriptions later in this document, breakdown tests are now rich with features. However, not all breakdown features of the fast WLR routines could be added without changing fundamental operation of the routines. Customers can license the fast WLR software to access the full set of Jramp and Vramp breakdown capabilities.

CMOS Problem Structure

Most instrumentation damage and testing problems seen at the customer site were traced to so-called oxide tests that caused the test structure to latchup. In an attempt to gain control over testing, voltage and current settings much greater than needed for oxide tests led to catastrophic destruction of the structure and left the test system in an uncontrolled state.

All of that was due to triggering of a multi-layer, PNPN, diode that would not turn off until applied voltage was reduced to the diode trigger or turn off level.

Test condition changes alleviated the problems, but changes to the software were needed to improve understanding and control of testing.

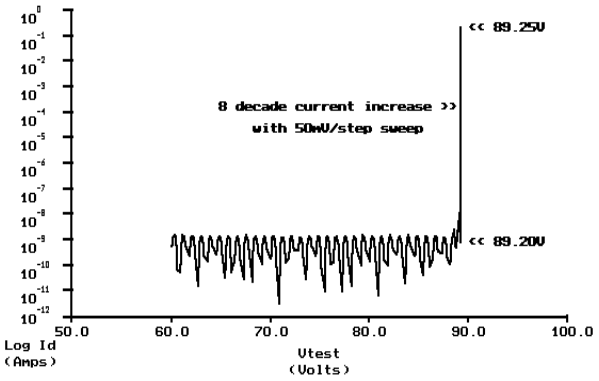

Figure 1 - Voltage vs. Current Sweep

The transformed EMAGE voltage versus current sweep in figure 1 shows a current increase from noise level of ~1nA to full DMM current of 200mA with a single 50mV step. With that much current, any oxide that might be in series with the structure was ruptured. Also, the sweep implies that current detection could be anything from a few nA to 200mA without affecting the breakdown voltage measurement.

Multiple layers of a MOS transistor made up the actual PNPN structure. In essence, CMOS latchup was being induced during the oxide test. Referring to figure 2, as test voltage Vt is increased, no current flows into the emitter of Q1 until Q1 or Q2 reach breakdown. If Q1 breakdown is lower, Q2 base current is multiplied by Q2 gain which causes Q1 to turn on. If Q2 breakdown is lower, Q1 action dominates. Regardless, little power is dissipated in Q1 or Q2 before they are fully turned on. As with CMOS latchup, limiting Vt current prevents damage.

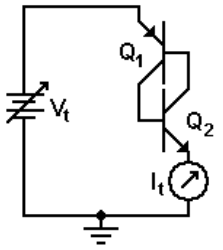

Figure 2 - Equivalent of PNPN Structure

Once turned on, the structure will not turn off until the Q1 base voltage is low enough to turn off Q1. For such a structure, there is no reason to have 10mA used for breakdown detection if that level results in testing problems. The lowest current/energy possible should be used to eliminate breakdown events that cause test system register scrambling and/or DUT damage.

Charging Unassigned Pins and Chuck

Because the bottom side of the PNPN structure was in ohmic connection to the wafer backside, it was also tied to the chuck. Thus, when the structure shorted, the chuck was brought to the forcing potential on the top side. If the chuck pin is not biased in the test, the PNPN structure turn-off voltage is left on the chuck after the test voltage is removed. Then the matrix pin that is connected to the chuck, and any other unassigned pin that might have been charged, is shorted to ground during power down. The energy from that discharge can be enough to scramble system registers and cause relays to weld. This was the testing sequence:

- DMM measurements showed a sharp current increase to ~5mA with 200mV steps.
- DMM input went to -40V when the device shorted.
- DMM input stayed at -40V with a 20kHz oscillation across the device for ~7msec.
- Control was regained and 10mA measured, the exit criteria, but the device was finally destroyed as evidenced by the oscillation stopping and the VFIF going into current limit at 100mA.

In conclusion, because the DMM was on the 10mA range, failure to detect the breakdown event led to 100mA flowing to another pin, probably the substrate/chuck, for ~7msec before the output voltage went to 0V after the DMM current came under control. It was surprising that registers were not scrambled for every device.

Fix ranging the DMM at 100mA allowed the device to short and destruct without losing instrumentation control, but that was hardly a foolproof solution.

For all breakdown tests involving this type of structure, test currents need to be reduced to the lowest acceptable level and all possible electrical connections to the structure need to be connected to a system resource.

- If voltages change with different test conditions, it must be due to inadequate characterization since the breakdown curve is so steep.
- If sneak paths are not identified and dealt with, there is no way for software to control energies involved with them.

Relaxation Oscillations

The behavior of the PNPN device allows it to become part of a relaxation oscillator whose frequency is dependent on the available current and system capacitance. The device is not damaged unless the test current is too high. However, setting the current higher does not stop the oscillation, it just raises the frequency if the VFIF providing the current can respond. If beyond the bandwidth of the VFIF, oscillation will occur as long as the output is current limited.

Figure 3 shows the PNPN structure with system capacitance C_S and a current limited supply. Charging rate (dV/dT) for the oscillation is simply the current I_L divided by capacitance C_S.

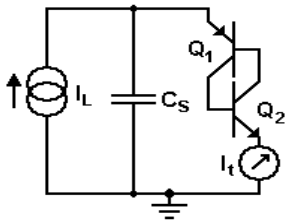

Figure 3 - Elements for Relaxation Oscillator

In the instance mentioned previously, oscillation was at 20kHz. In another case, oscillation was ~600kHz with a charging signal of 30V/2µsec at ~10mA. That is consistent with unguarded system capacitance of 350pF.

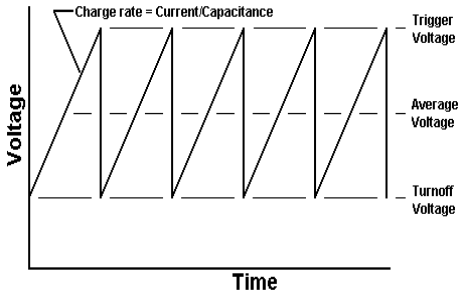

Figure 4 - Relaxation Oscillation Illustration

Figure 4 illustrates what would be seen on an oscilloscope monitoring the VFIF output. Turn off voltage is shown above 0V because that actually happened at the customer site, and is expected if the driving current I_L is enough greater than the test current I_t that the meter input is pulled away from ground.

Effect on VFIF Operation

Relaxation oscillation had an unforeseen effect on VFIF operation. Note that in figure 4, the average is well above 0V even with a turn off voltage near 0V.

The unforeseen consequence was that VFIF output responded to the average value when the power down routine reduced the VFIF current to 0A, and that drove the sense buffer, and/or the current sense buffer, beyond the common mode recovery voltage of the operational amplifiers in the VFIF.

Figure 5 of the voltage versus time plot of the PNPN structure shows charging up to breakdown, a sharp drop at breakdown, and the average value of the resultant oscillation. The sawtooth in figure 4 is not seen because DMM bandwidth was not high enough to respond to the 600kHz oscillation.

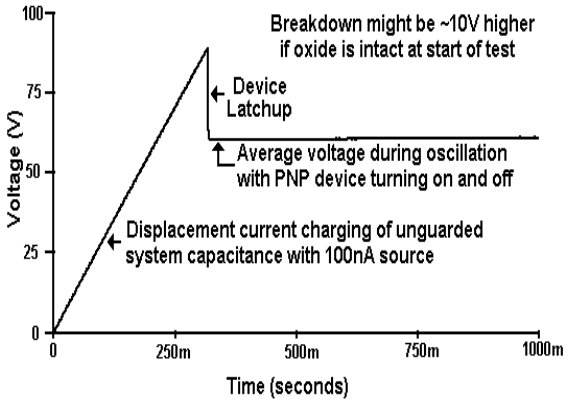

Figure 5 - EMAGE Voltage vs. Time Plot

Since it takes relatively little current to pull the supply out of latchup, and since grounding all nodes does not do the job with 1µA as current limit, the solution is to increase the current to 100µA prior to power down and set the VFIF voltage to zero.

Bipolar Transistor Breakdown

If breakdown, or maximum operating voltage, tests do not cause parasitic structures to trigger, instrument control is seldom lost. Higher voltage breakdowns with 2kV sources have enough energy to cause instrumentation register scrambling, so scrambling detection and recovery was added to those test types.

Until late in 2009, instrument aborts and random reed relay welding had been attributed to sneak paths such as the one described earlier. However, a customer running a conventional bipolar process had troubles with aborts when testing planar NPN vertical transistors with no possible sneak paths. Investigation at the customer site using scrambling detection software proved that scrambling was occurring with BVceo breakdowns approaching 100V. Subsequently, extensive software changes were made to reduce effects of bipolar breakdown and to recover instrument control.

Initial Test Vehicle

A leaded 2N3904 was used to successfully induce breakdown register scrambling. Biasing the base with a voltage source brought transistor turn-on below 100V. Figure 7 shows testing results before making changes.

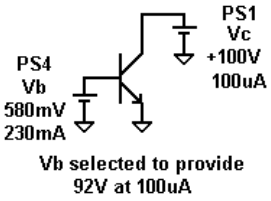

Figure 6 - BVcev

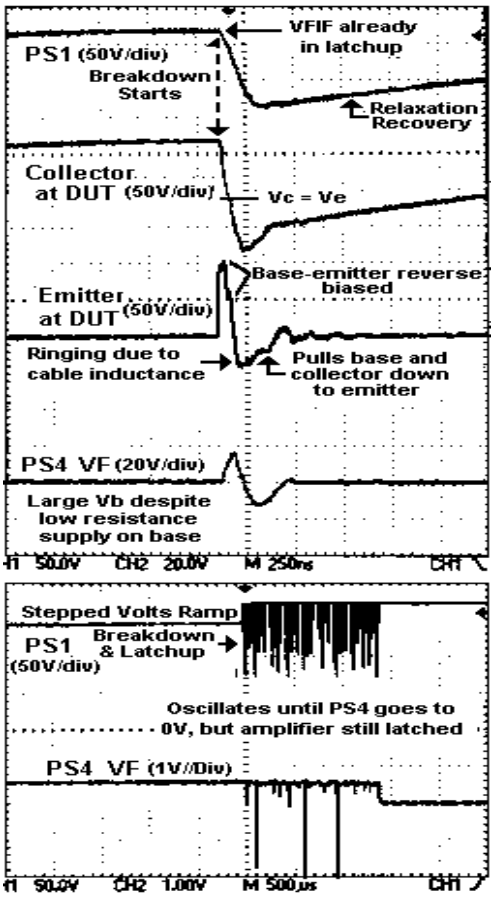

Figure 7 - Oscilloscope Captures of BVcev

Effects of Bipolar Breakdown

The composite set of events in figure 7 illustrate how fast the breakdown is, that seemingly solid ground and power supply connections are driven to ±50V, that the principal supply is being driven into a latchup state by the breakdown, and that relaxation oscillation continues until the base is turned off.

In capturing the events, aborts were seen to have a different character than those seen during 2kV testing. That is, with 2kV testing, many registers were scrambled throughout the map, leading to the conclusion that digital ground currents directly affected contents of data latches. At <100V, aborts are:

- Largely confined to modules used in the test.
- Often caused by errors in data being read. For example, a ReadHdw will indicate that a relay is closed when a subsequent memory map proves otherwise. This leads to aborts about Ilimit checking being invalid if a module is not connected and to FindDACrange aborts.

Abort and scrambling detection code developed for 2kV testing reliably detected breakdown and was a boon in the bipolar breakdown investigation. A key ingredient is the memory mapped control.

Types of High Energy Bipolar Breakdowns

As noted in the diagram below, transistor action multiplies the injected charge and makes the transistor conduct at much lower voltage than true BVcbo and does with regenerative feedback that behaves like negative resistance.

Even a BVcbo measurement involves a parasitic path for emitter current into the emitter cabling capacitance.

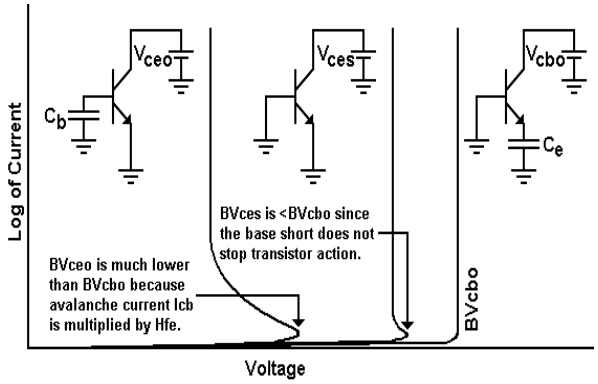

Figure 8 - High Energy Bipolar Breakdowns

Memory Mapped I/O Control

In Reedholm systems, modular instruments plug into an analog/digital back plane without slot dependence. That is, any module can go into any slot as long as the cabling that connects the instrument to the outside world can reach it. Manual DIP switches set each address. Most modules contain 64 bits of address space that hold instrumentation control information, measurements, and Boolean flags.

Menu-driven troubleshooting software allows investigation of the instrumentation status at any time as shown the figure 9 memory map. In the map, cross Point Matrix (CPM) #1 is at 00h, #2 is at 08h, etc. Each hexadecimal address location shows the contents of one byte in hex code. The 256 locations shown in the map contain 2048 bits of data.

There are no microprocessors or state machines to interfere with this flat hierarchy of direct instrument control. As a result, this approach provides excellent system characteristics:

- Maximum system control because all states can be directly controlled. Unlike other complex systems that can lose communications with controlling software, Reedholm instrumentation never gets in a state that one has to power down to regain control.
- Highest possible speed because each and every register can be directly read from, or written to, without going through a prior sequence.
- Detection of, and recovery from, loss of control when high energy noise from voltage breakdown flows through the instrumentation. By reading the memory map before high voltage and breakdown tests, changes to the map are detected and the original value are restored in 400µsec, well before relays have a chance to change state. Thus, breakdown events are detected if missed by the measurement code.

```
**************************************************************************
 Instrumentation Memory Map:   MemBase =       Group = 0
**************************************************************************
2nd Adx Char ---->   0  1  2  3  4  5  6  7    8  9  A  B  C  D  E  F
1st Adx Char -> 0   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 1   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 2   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 3   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 4   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 5   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 6   48 01 7F F7 10 02 FF 00   20 01 7F F7 10 02 FF 00
1st Adx Char -> 7   4C 01 7F F7 10 02 FF 00   5F 01 7F F7 04 00 00 00
1st Adx Char -> 8   00 29 7D 00 00 00 01 00   00 42 00 00 20 00 01 00
1st Adx Char -> 9   00 18 00 00 00 00 00 00   73 21 7F FF 00 5C 6C 00
1st Adx Char -> A   50 54 45 54 2E 4F 3B 00   00 00 00 00 00 00 00 00
1st Adx Char -> B   3B 04 7F F7 10 00 00 00   57 04 7F FF 04 00 00 00
1st Adx Char -> C   00 84 00 00 00 00 00 00   00 84 00 00 00 00 00 00
1st Adx Char -> D   00 84 00 00 00 00 00 00   00 84 00 00 00 00 00 00
1st Adx Char -> E   00 00 00 00 00 00 00 00   00 7F FF 00 00 00 03 30
1st Adx Char -> F   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 38
```

Figure 9 - Function Cage Memory Map

Coupling Edges to Relay Coils

Most, if not all, false reads are due to breakdown events being capacitively coupled to relay coils while relays are off. Thus, false node detections are of nodes that appear to be connected but are never of nodes appearing open when they are not. Similarly, most FindDACrange aborts are caused by too many range relays being called or set.

However, some FindDACrange aborts happen when breakdown events couple to the Clear line used by 12-bit modules. A DMM-16 ECR places a 10nF capacitor on that line so that it no longer reacts to breakdown events.

Figure 10 is of relaxation oscillation during a BVcev test prior to instrumentation hardware changes. The steep lines are 100V+ breakdowns with <100nsec transition time, and each one couples enough voltage to cause false readings when relay control registers are interrogated.

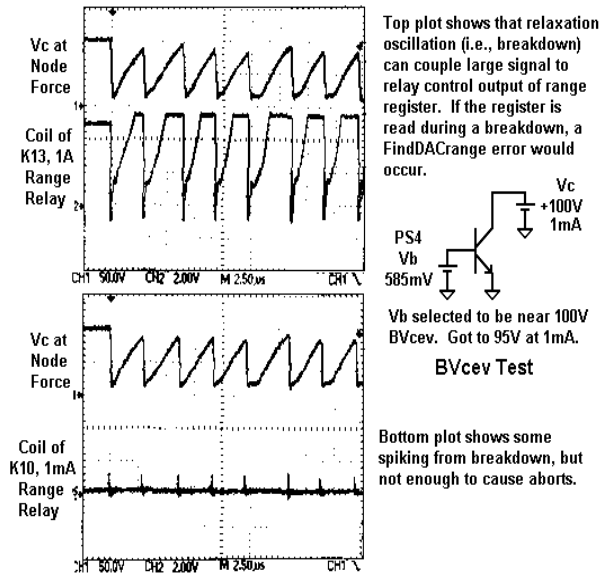

Figure 10 - Coupling to Relay Coils

Relaxation Oscillation is Breakdown Train

While the relaxation oscillation depicted in figure 3 are of a parasitic CMOS device, bipolar transistor breakdown typically results in relaxation oscillations without requiring parasitic connections or destruction of insulating layers.

At the first breakdown, the collector-base diode avalanches, injecting charge into the base which causes transistor action that accelerates breakdown to very high speeds.

The BVcev breakdown shown in figure 11 is a comparison between what happens with upgraded VFIF-16 modules and unmodified VFIF-12 ones. Although the VFIF-16 has four bits more resolution and slightly different internals than a VFIF-12, it is identical operationally during breakdown measurements.

Testing with the VFIF-16 terminates when it should based on input delay and having reached the target current. However, one, or both, of the VFIF-12 buffer amplifiers latched up at the first breakdown, and stayed latched up at the end of the input delay. A 100msec recovery ensued while software regained control.

During latchup, the VFIF-12 amplifiers supplied much higher recovery, or recharge, current than implied by the programmed current. As a result, oscillation frequency was much higher than with the upgraded VFIF-16. Each relaxation cycle includes a breakdown event with the same energy as the initial one regardless of the recharge current, so the VFIF-12 modules produced 8,000 breakdown events per test while the VFIF-16 modules only had six. Since each breakdown can induce scrambling, the unmodified VFIF modules have >1,000 times higher likelihood of causing an abort.

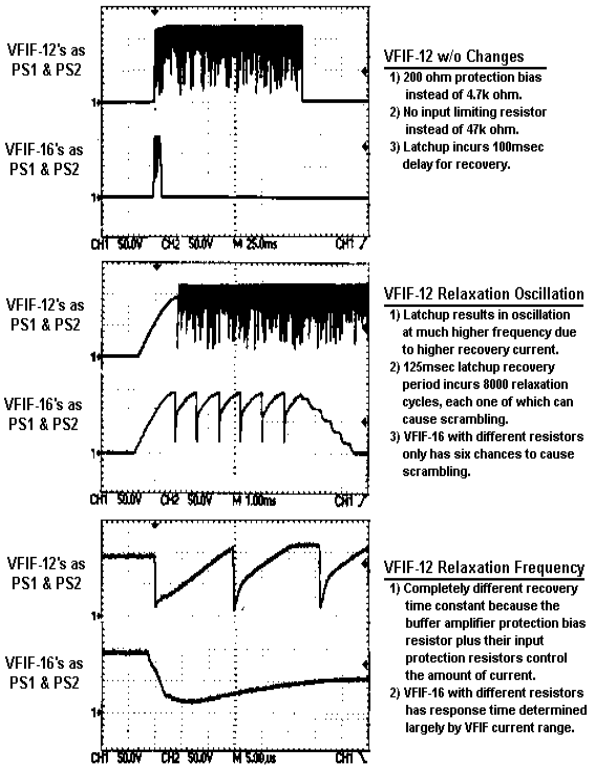

Figure 11 - Upgrade Effect on Relaxation Oscillation

Latchup of Apex Op Amps

If the non-inverting input of an Apex op amp used for buffering is driven fast enough to either voltage supply (+120V or -120V), control from the non-inverting input is lost and the gain from the inverting input is inverted. That causes the op amp output to be latched at +120V or -120V. If the input to the op amp is opened at that point in time, the op amp stays in a latched condition indefinitely. For testing, it is possible to induce latchup by touching the non-inverting input to either supply through a 51kΩ resistor.

Figure 12 is from the Apex data sheet with values critical to latchup analysis added. The schematic diagram of the VFIF-16 sense buffer and DMM-16 input buffer is shown immediately below with upgraded resistor values. The ±105V labels indicate protection clamps for 2kV operation.

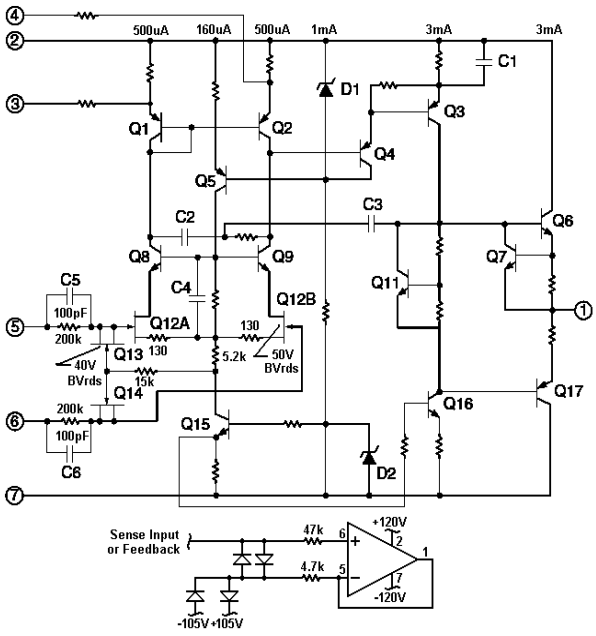

Figure 12 - Apex PA82J & Use in Buffer Amplifier

Apex Gain Inversion

The inversion appears to happen for fast negative voltages mainly because the input capacitors are relatively large and behave like short circuits for fast edge signals. Thus, a fast 100V signal is not clamped by input protection offered by Q13 and Q14, but goes through to the differential transistor Q12 causing it to breakdown. Thus, for signals above –50V, breakdown of Q12B from gate to drain steals current from Q12A and causes the output to go to +120V.

Recovering From Latchup

Bringing the op amp out of latchup requires sinking the current that flows through the input stage transistor gate, series resistors, and protection diodes. If the non-inverting input is pulled 20V away from the latchup voltage, i.e., to ±100V, the op amp recovers.

VFIF Latchup Recovery

Two buffer op amps are attached essentially to the same point in the VFIF, but serve different functions: one drives the current mode feedback path and the other drives the voltage feedback resistor. Either can latchup and drive the load current while latched up. However, no current flows to or from the VFIF non-inverting input during latchup, so the only chance for system damage is opening or closing a switch in series with the VFIF output.

- When latched up, the Vzero bit is False and the Ilimit bit is True. Thus, if Vzero is true after attempting to power down, damage cannot occur from opening VFIF connections. If Vzero is False, the latchup recovery described next should result in making Vzero true.
- Setting the VFIF to 100mA on the 100mA range pulls it of latchup because the output amplifier can control the overall feedback loop through its 50Ω range resistor. The 500Ω resistor on the 10mA range is also low enough, but takes longer.

DMM Latchup

There are three sense buffers in the DMM. The current mode meter high buffer cannot latchup because there is a current path back through the feedback resistors plus loading on the output that precludes latchup. Thus, the only concerns are with the meter low buffer used for voltage and current modes plus the meter high voltage buffer.

If in current mode, latchup cannot happen if meter low is grounded, but can if meter low is biased and if the bias supply is latched up or at high voltage. Also, if in voltage mode, the meter low buffer can be latched up if it is biased.

If meter low is already tied to node 0, even if by scrambling, it is not disconnected. Otherwise, the buffer could latchup and/or node 0 relay could weld. If tied to a node with another module, bringing those modules to 0V protects the buffers plus external relays tied to them.

- If tied to a VF, SCM, PPG-4, or HISMU, any of those modules prevent latchup because of their voltage limitations. Thus, when they power down, MH or ML would be brought to 0V also.
- If tied to VFIF, VFIF latchup recovery pulls the DMM buffers to 0V.

DMM Latchup Detection

Unfortunately, there is no Vzero or Ilimit hardware detection on the DMM-16, so the state of those bits cannot be used as they can with a VFIF. Thus, there is no direct way of knowing if latchup has happened. Being overscale is not enough of a warning although that is used for the current limit flag.

DMM Latchup Recovery

If tied to an open node, or to a module without sufficient current sinking, input buffers can be pulled out of latchup by connecting to a node. In addition, they can be pulled into operation by changing modes. After other modules are returned to 0V, switching between current and voltage modes with a short delay between modes is enough. When the DMM is in current mode, voltages going into the differential stage are near zero, so switching to voltage mode instantaneously pulls a lot of current to charge the few tens of pF of internal DMM capacitance load. Then the DMM is left in current mode to prevent node charging.

Stepped Voltage Tests

These tests step voltage from a start value until a target current or an endpoint voltage is reached. Voltage at the target current is returned unless the endpoint is reached without the target current being detected. However, the test error in that case can be converted from 1E+20 if the option is selected to return the endpoint voltage instead of the encoded error.

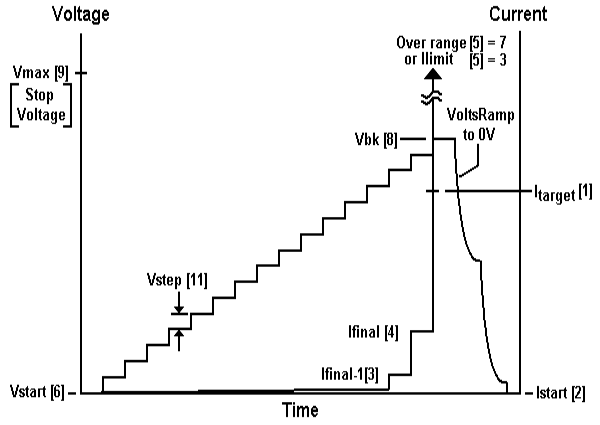

Figure 13 - Stepped Voltage Ramp Parameters

Prior to starting the ramp, the greater of the start and end point voltages is used to fix the voltage range and set ramp direction. A HVSMU is automatically used if the start or stop voltage is >100V.

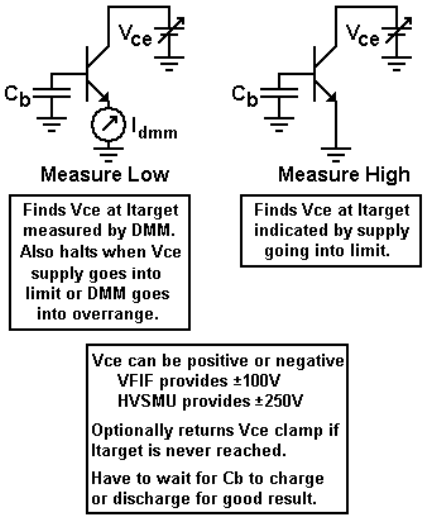

Figure 14 - BVceo with Stepped Voltage Routine

When the HVSMU is used, test currents are rounded up to cardinal values of 1µA, 10µA, 100µA, 1mA, and 10mA. Sensing in the low lead is done with the attached meter that can be the DMM or HISMU. This has the benefit of using digital averaging to reduce noise contribution at low currents.

Test Engine Breakdown Routine

The EMPAC/Build breakdown routine contains stepped voltage tests that are now true breakdown tests instead of just finding voltage at a current.

- Ramp will not start if any supply is in limit when it should not be and will halt if any supply goes into limit when it should not. If breakdown detection is turned on, any supply going into limit is considered valid termination and the result set to the voltage at that point.
- Current values are not absolute so that a breakdown can be detected in the base of a transistor when polarity switches.
- If the DMM goes into over range in either direction, the ramp is terminated.
- The type of termination is encoded and likely voltage stored in the RIresults array.

Current Limit Checking

The current limit checking routine provides unambiguous reporting of the reason for test termination. Versions prior to adding breakdown features had the last invalid limit condition overwrite preceding events that could be considered breakdown indicators. Limit checking starts with PS#1 and progresses through PS4. The test terminates as soon as a supply was found to be in limit. All supplies connected to nodes are checked, including the HISMU.

Limitations in Final RDS DOS Version

RDS DOS limitations compared to RDS Intranet:

- Can only do 200V test starting at -100V instead of any voltage between –100V and +100V.
- Can have stepped voltage breakdown to +250V, but cannot force I measure V to ±250V.
- Can only use DMM for force I or V tests.

Errors and RIresults Array

The next page provides details on the error reporting, handling of current limit, types of test termination now available, and assignments of RIresults.

Stepped Voltage Tests

Error Reporting and Limit Checking

Instrument conditions are monitored to assure satisfactory results. When they occur, test errors are encoded and multiplied by 1E+20:

Code	Error Description
1)	Target current not found.
2)	PS1 is in current limit.
17)	Step or start voltages beyond range.
19)	PS3 is in current limit.
20)	PS4 is in current limit.
38)	DMM was overranged.
39)	PS2 is in current limit.

RIresults Array

RIresult[5] categories identify the type of ramp termination. Types 3, 5, 8, and 9 probably qualify as valid breakdown events with type 8 being the most desirable. For those types, the final voltage in RIresult[8] could be used as the breakdown voltage. Types 1, 2, 4, 6, and 7 mean the test did not start or breakdown was not reached. Calc3 could be used to convert the result if breakdown was not reached. Otherwise, results from those types should be discarded.

Results 7 and 10 to 12 are mainly used for test code troubleshooting. The test result assignment was not altered, but information was generated to make the test more useful for breakdown measurements.

Element	Contents
1)	Target current (CalcSeven if current measured).
2)	Initial current, if measured, at start of ramp.
3)	Current, if measured, on next to last step.
4)	Current, if measured, on last step.
5)	Type of test termination: 1: Test not started because of setup data problems. 2: Stepping supply in limit at first voltage. 3: Stepping supply in limit during ramp. 4: One or more supplies in limit at first voltage. 5: Some other supply went into limit during ramp. 6: Stop voltage reached w/o planned finish. If Calc3 = 1, test result is changed to stop voltage. 7: Current exceeded meter range at 1st voltage. 8: Planned ramp finish from limit bit or current measure. 9: Current measurement exceeded meter range during ramp. 10: Instrumentation abort detected.
6)	Starting voltage (PS1_Voltage).
7)	Starting voltage in lsb's (mainly for troubleshooting code).
8)	Voltage causing ramp termination.
9)	Maximum or stop voltage (CalcOne).
10)	Stop voltage modified for comparison.
11)	Step voltage (CalcTwo).
12)	Step voltage in lsb's (mainly for troubleshooting code).

Force I, Measure V Tests

These tests force a current into a pin and measure resulting voltage relative to ground with the DMM. With changes made in March 2008 and February 2010, these tests are faster and as precise as the slower stepped voltage breakdown tests.

Test Engine V @ I Routine

The EMPAC/Build V @ I test engine routine is at the heart of the force I measure V breakdown tests. Changes to the force I test let it be used as a quasi-ramp instead of having to use the stepped voltage tests to find the voltage causing a device to breakdown. Because the V @ I routine also provides current measurement, that test type can be used as a quasi-ramp for current. Breakdown test features include:

- Power supply limit checking described in the stepped voltage breakdown section.
- Instead of using a delay function, measurements are continually made while the test settles to a value. Low level timing primitives are used to assure that settling time is properly measured.
- The type of termination is encoded and several candidates for breakdown voltage or current are stored in the RIresults array.

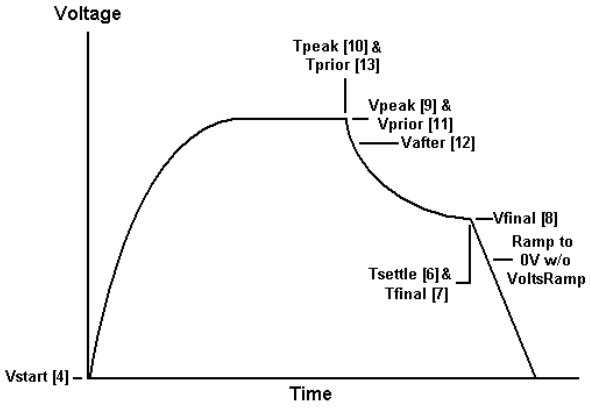

Figure 15 - Force I, Measure V Parameters

Stress at Is

This test ties the low pin to analog return because the test is not intended for use with large currents at low voltages. Stress current can be applied indefinitely with stress time entered in seconds. The voltage after initial delay plus calculated slew delay is stored in RIresults[2], after which stress time starts. Voltage at the end of stress time is stored in RIresults[3], and actual stress time is stored in RIresults[1].

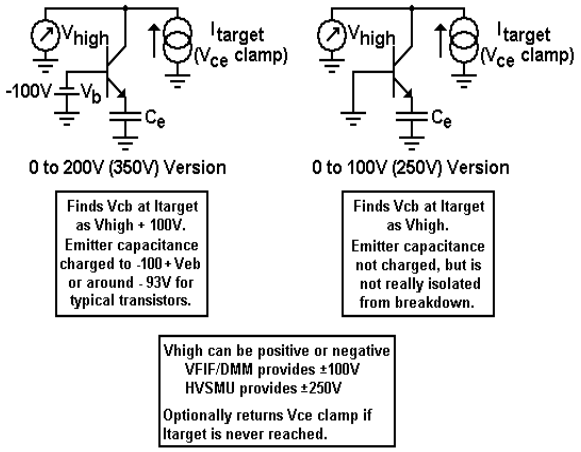

Figure 16 - BVcbo with Force I Routine

The image above shows connections for BVcbo measurements with the force I, measure V routines. Note that the emitter capacitor is a parasitic element.

Improved Accuracy at Higher Currents

Biasing the low pin at 0V is the default to sense voltage at the low pin and keep it close to 0V (i.e., within the SelfCal voltage offset of PS3 used for biasing the low pin). Not biasing the low pin causes a voltage on the low pin due to the test current flowing through the cable resistance in series with node 0 matrix relay resistance. At low currents, that voltage is insignificant, but with a return path resistance of 400mΩ, 10mA would produce 4mV. With SelfCal, offset of the low pin supply is corrected within 0.5 of an lsb (least significant bit). Thus, a 12-bit supply would have error <625µV, and a 16-bit one <39µV immediately after SelfCal is applied.

200V Breakdown

This breakdown test biases the low pin at –100V using PS2. Since intended for devices that breakdown between 100V and 200V, the query is for voltage >100V. However, device breakdown is returned for values between 0V (PS1 at –100V) to 200V (PS1 at +100V). PS2 supplies a bias condition of –100V at a maximum current of 200mA. That current must be set higher than the test current from PS1 to make sure that PS2 output voltage is not pulled higher than –100V. The DMM range is set to the voltage compliance beyond 100V. An option exists to return voltage clamp if reached. If enabled, the maximum PS1 voltage (or PS1 voltage plus 100V for the 200V test) is returned instead of the encoded error for PS1 not being in current limit. The HVSMU cannot be used for force I, measure V tests in RDS DOS.

200V BVcbo After Hardware Upgrades

The image below is of a BVcbo test after the DMM-16 and VFIF-16 resistor changes that reduce latchup. It shows timing relationships as well as hard turn-on of the transistor during power-down.

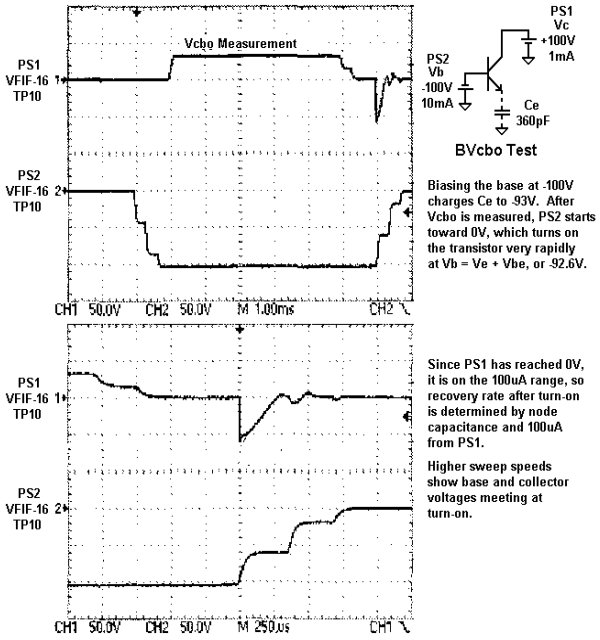

Figure 17 - 200V BVcbo After Hardware Upgrades

Ramp Test with Termination

Measurements are continuously made instead of using delays to gather data through breakdown. The test result is not set until initial delay plus calculated slew delay is reached. As noted on the previous page, the Stress at Is test assigns that voltage as the first voltage under stress. Prior to that assignment, measurements are continually taken and current limit bits checked for all supplies. Furthermore, the absolute value of the measured parameter is kept as a peak detection so that a 15% inflection in voltage or current can be interpreted as a possible breakdown event. For the Stress at Is test, time is continually monitored while taking data so that the test terminates when the stress time elapses.

Devices that do not short or open will be at the breakdown voltage at the end of the test. For shorted or open devices, the RIresults array can be used to return the last voltage before breakdown.

Errors and RIresults Array

The next page provides details on the error reporting, handling of current limit, types of test termination now available, and assignments of RIresults.

Force I or Force V Two Terminal Tests

Error Reporting and Limit Checking

Instrument conditions are monitored to assure satisfactory results. When they occur, test errors are encoded and multiplied by 1E+20:

Code	Error Description
1)	Forcing supply PS1 did not go into current limit
2)	If not overridden by return clamp, PS2 is in current limit.
19)	PS3 is in current limit.
20)	PS4 is in current limit.
38)	DMM was overranged.

Ctrl Pin bias is provided with PS2 for tests other than 200V breakdown, and can be used to force current or voltage. CalcSix as displayed on the Help Status screen is used to modify interpretation of the PS2 limit bit. This modification of the PS2 limit bit meaning applies to the force V measure I tests as well.

Value	Meaning
1)	Force voltage, error if in current limit
2)	Force current, error if not in current limit
3)	Force current, ignore current limit
Blank)	Force voltage, ignore current limit

RIresults Array

RIresult[5] categories identify the type of ramp termination. Types 3, 5, 8, and 9 probably qualify as valid breakdown events with type 8 being the most desirable. For those types, the final voltage in RIresult[8] could be used as the breakdown voltage. Types 2, 4, 6, and 7 mean the test did not start or breakdown was not reached. Calc3 could be used to convert the result if breakdown was not reached. Otherwise, results from those types should be discarded.

Element	Contents
1)	Time under stress starting at settling delay which is the sum of initial and calculated slew delay.
2)	First voltage or current after settling delay.
3)	V or I at end of elapsed time (last V or I).
4)	V or I at start of test.
5)	Type of test termination 2: Forcing supply current limit bit invalid at start. 3: Forcing supply current limit bit invalid after start. 4: One or more of other supplies in limit at start. 5: Some other supply went into limit after start. 6: Reached final time with forcing supply limit invalid. 7: V or I measurement exceeded meter range at start. 8: Reached final time with forcing supply still in limit. 9: V or I measurement exceeded meter range after start. 10: Instrumentation abort occurred.
6)	Time after settling delay.
7)	Time at termination.
8)	V or I right at or before termination.
9)	Peak V or I excluding overrange or termination.
10)	Time at peak V or I.
11)	V or I before 1st 15% increase or decrease.
12)	V or I after 1st 15% increase or decrease.
13)	Time to 1st 15% increase or decrease.