

Device Degradation Reliability Analyzer

Model RI-53

- Comprehensive Stress/Test Selections
- In Situ Characterization
- Selectable Temperature Ramp Control
- Uncompromised Oven Performance
- Simple, Rugged Oven Interface
- Guarded, Shielded Leads
- 1°C Load Board Uniformity Span
- Accurate, Unambiguous Data
- Open ASCII Data Files
- PC and Tester Error Recoveries

The RI-53 combines a fully integrated reliability test environment with excellent measurement quality and sensitivity. This makes it an ideal device degradation reliability test system for process development, qualification, and monitoring.

Temperature Control

The hardware and software supplied with the RI-53 address several areas of concern regarding temperature uniformity and control:

- **Load Board Temperature Uniformity**
The cabling for stress voltage delivery and DUT monitoring is routed through the purge hole in the thermal chamber. This is a significant improvement over alternative approaches that compromise temperature uniformity by using modified thermal chamber doors. Routing the cables through the purge hole reduces the load board temperature span to 1°C.
- **Temperature Ramp Rate**
Fast temperature ramp rates usually cause thermal overshoot. Overshoot and rapid temperature changes can potentially over stress load boards, connectors, and test structures. Reedholm applications software eliminates this problem by allowing user defined ramp rates.



- **Device Temperature Stabilization**
Another software feature uses a "soak time" to ensure that all devices have reached the desired temperature. After the thermal chamber reaches the target temperature, a user specified time elapses before stressing begins.

Access to Test Data

To ensure data is easily accessible, the RI-53 stores all test result data in well documented ASCII file formats. Also, the option to output data into dBase IV format is available. Both ASCII and dBase IV files can be easily imported by many third party analysis tools, whether local or residing on a network resource.

PC Based Control and Connectivity

The RI-53 system is controlled by the latest generation of personal computers with memory mapped interfaces that enable communication between the computer and the instruments in less than 10µs.

Connecting the controlling computer to a network for data storage is easy and also provides automatic data archiving. Reedholm's site license software policy provides a distributed test environment, allowing test plans and data to be manipulated on multiple computers.

Transistor Monitoring

The desired stress voltage(s) are provided in parallel to each of the devices in an experiment. A separate stress supply can be attached to each of four device terminals, with a fifth grounded. A measurement cycle or scan is performed by sequentially executing a series of user defined tests on each device remaining in an experiment. The stress power supplies provide up to 1A of stress current at up to 10V or 100mA of stress current at up to 100V. These current limits should be sufficient to maintain the stress level even if one or more devices become shorted. If not, optional series resistors can be included. In sequence, the test algorithm:

- Periodically stresses, measures, records results, and disconnects failed devices.
- Optionally scans without storing results.
- Terminates when specified criteria are met.

Infant Scans

At the start of an experiment, infant scan(s) are performed so that all devices can be proven functional. The first scan is done at ambient temperature, after which any defective material can be replaced and the scan repeated. The failure criteria used during the infant scans can be different than the failure criteria used in the experiment.

Once the thermal chamber has reached the stress temperature, another infant scan is performed. Again, the user has the option to replace the failing devices and re-

test. However, at high temperature this may not be practical unless all devices fail.

Normal Scans

Logarithmically, linearly, or at a user specified frequency, a normal scan occurs and the test results are stored. After the scan, any failed devices are disconnected from the stress supplies.

“No Data” Scans

The software provides an option to perform scans in between the normal scans, termed “no data” scans. After the measured parameters increase above the noise threshold of the test system, results of “no data” scans are stored when either of the two events occurs:

- A device exceeds the failing limits specified.
- A test result shifts by a specified amount.

Failed devices are also disconnected from the stress after “no data” scans.

Post Scans

In addition to infant and normal scans, post scans can be executed after an experiment has finished. This allows data to be gathered at different temperatures and compared to the infant data. During a post scan, all devices that did not fail the infant scans are tested.

Applications Software

EMREL is the interactive software tool used to perform stressing and monitoring on the RI-53. It can control up to six independent experiments and is used for:

- Setting up and starting experiments.
- Performing scans on active experiments.
- Viewing logs and reports.
- Creating graphical representations of results.

Another EMREL feature allows the following information to be recorded for each device, enabling test results to be tracked to their origin:

- Lot identification and wafer number.
- Die name and X and Y location.

EMPAC is used to create the test plans executed during each scan. Each EMPAC test returns one test result. Examples of EMPAC test types are voltage threshold, transconductance, linear and saturated drain current, etc. The large library of standard test types can be augmented by user written tests and equations.

EMAGE is used for test setup when either sweeps of I/V data or in situ characterization are desired. EMAGE is also used to display and analyze EMREL’s graphical summary reports.

The combination of EMPAC and EMAGE test types provides an unlimited flexibility in both the number and type of test parameters used. Each scan can literally execute anywhere from one to hundreds of tests in between stressing. Separate data sheets exist for both EMPAC and EMAGE.

Error Recovery

In order to prevent data loss, the system software can recover from error conditions while experiments are active. At a minimum, the software allows the experiments to be continued. Some of the error conditions the software can recover from are:

• Loss of Computer Power

If the computer is turned off, or when the instrumentation is being used for diagnostic testing, scans cannot be performed. Once the Reedholm shell is restarted, all active experiments are checked. Stress levels are maintained during the time the computer is not available.

• Loss of Tester Power

EMREL continuously monitors the voltage stress status for each active experiment and periodically checks all hardware. If any stress supplies or matrix pins are not set correctly, EMREL suspends the associated experiment, powers down its stresses, and unhooks its matrix pins. A single attempt is made to reset the experiment. If unsuccessful, it is powered down and flagged on screen with an error message.

• Loss of Experiment Scheduler

Control of all experiments is handled using two schedule files. If these files are accidentally deleted or corrupted, EMREL can rebuild them using the stored test data. This rebuilding permits experiments to be restarted, even if the test computer has to be replaced.

Experiment Setup

Prior to starting an experiment, an input grid is filled in as shown in Figures 1 and 2. Along with a few optional cells at the top, the HCI input grid contains sub-sections for the following parameters:

- General Setup Parameters**
 The experiment bank number being used is entered along with the number of devices and the matrix pin to device terminal translation table.
- Time Parameters**
 The time parameters include the experiment duration, the initial stress time between scans, and a multiplier used to set a log or linear stress time step. In addition, the thermal stabilization time is included.

- Stress Parameters**
 The stress parameters include the stress temperature and voltages used to accelerate the failure mechanism. The temperature ramp rate is also included.
- Test Parameters**
 The test parameters are simply the EMPAC and optional EMAGE test plans to be used, along with the frequency to perform the EMAGE tests. EMAGE tests can be scheduled to occur at the start of each experiment and when each device fails, along with additional intermediate times.

The TDDDB grid is described in the RI-51 data sheet.

Comment		0.25 Evaluation		Tracking	
Operator		McKenney		Facility Fab 10	
Hot Carrier 2		Process CMOS A25		Structure 74N	
General Setup Parameters					
Bank	1	Devices	8	Temp Off	N
Pin Table		HCI4007			
Time Parameters					
Length	100	Delay	300	Multiplier	
Soak		60			
Stress Parameters					
Temperature	75	Stress U1	3.3	Stress U2	1.15
Ramp Rate	3	Stress U3	100n	Stress U4	0
Test Parameters					
EMPAC Test Plan	4007TST				
EMAGE Test Plan	4007_HCI				
Sweep Per Scan	10th Scan				

Figure 1 - EMREL Hot Carrier Input Grid

Comment		0.25 oxide evaluation		Tracking	
Operator		McKenney		Facility Fab 10	
TDDB Multiple 2		Process CMOS A25		Structure 68L	
General Setup Parameters					
Bank	2	Devices	35	Temp Off	N
PINS:		Stress	24	2nd/Unused	48
Unused		<input type="checkbox"/>			
GND/Unused		<input type="checkbox"/>			
Time Parameters					
Length	500	Delay	600	Multiplier	
Soak		60			
Stress Parameters					
Temp.	200	Voltage	3.3	Ramp Rate	3
Test/Fail Parameters					
Stress Fail I	30m	Cap Area		Cap Thick	
Infant Fail I	100n	1st Test U	1.2	1st Test Dly	15
Test Fail I	15m	2nd Test U	-1.2	2nd Test Dly	15
Test Jump I	10	3rd Test U	-0.8	3rd Test Dly	15
Noise I Lvl	100p	4th Test U		4th Test Dly	
Stress Dly	10				

Figure 2 - EMREL TDDDB Input Grid

System Elements

Instrument Enclosure

For a standard configuration, the RI-53 enclosure is a 7-foot, mobile rack with separate card files for switching matrices, instrumentation, and stress supplies. The test computer and printer are placed on a table adjacent to the instrumentation chassis. To accommodate the stress supplies needed for the dual stress supply configuration, external stress chassis may be required.

Inside the test system, static power units provide dc voltages to the matrix and instrument backplanes.

Switching Matrices

The architecture of the RI-53 is one in which each experiment uses a separate matrix bank. Banks contain one to six crosspoint matrix modules (8 to 48 matrix pins). The maximum number of devices that can be tested in each bank is a function of how many independent terminals are required per device. When separate pins are required for stresses on the source, gate, drain, substrate, and well terminals, with one of the terminals grounded, each bank can test a minimum of a single device to a maximum of eight devices. If only a single stress level is required, the maximum devices per bank increases to 24 for HCI testing. However, TDDB testing can also be done, increasing the device count to 46 per bank. While the base system consists of two fully populated matrix banks, the maximum configuration contains six banks.

The high quality dry reed relays used on the matrix modules provide the optimal combination of signal transmission, pin isolation, and life expectancy.

Stress Supplies

Up to four supplies are used to simultaneously stress all devices in a given experiment. Each supply is a programmable, bipolar voltage source that can provide a nominal load current of 1A at a maximum output voltage of $\pm 10V$ with respect to ground. A second option for stress is a supply that can provide a nominal load current of 100mA at a maximum output voltage of 100V with respect to ground. The analog circuitry consists of a high-gain, high-voltage, FET input operational amplifier followed by a power output stage. The voltage reference for the stress supply is a 16-bit precision D/A converter that outputs voltage on three different ranges, with $78\mu V$ resolution on the lowest range. A three-pole switch connects the supplies to the analog cabling. This switch allows for the accuracy enhancing feature of Kelvin sensing within a fully encompassing driven shield. Although the voltage source can supply its maximum current to a load, it is fully protected against indefinite output short circuits. Systems can be delivered with the low voltage or high voltage stress modules or both types.

Measurement Instrumentation

Devices are measured in sequence using programmable voltage/current sources and a digital multimeter. Current is measured using an active metering technique that provides almost zero voltage burden while measuring currents up to $\pm 200mA$. This means that the meter can be assumed to be an ideal zero-ohm and zero-volt short on each of the eight current ranges until current limiting occurs.

Voltage is measured, with a resolution of $< 8\mu V$ on the lowest voltage range, by the precision voltmeter that has a differential input stage with each input terminal having an effective input resistance of $100G\Omega$. Both inputs operate linearly over the dc range of $\pm 100V$. Because the common mode rejection ratio (CMRR) is 106db, small differences in voltage can be measured with $< 5\mu V/V$ uncertainty due to CMRR.

The meter uses a monolithic, 16-bit sampling, A/D converter based on a successive approximation algorithm. During system initialization, a self-linearizing calibration routine automatically executes and produces full 16-bit linearity. For maximum sensitivity, the digital averaging feature of the low level instrument drivers provides repeatable sensitivities of $\pm 2pA$.

In addition to the digital meter, programmable voltage/current sources provide bias to the gate, drain, source, and substrate terminals of each device. This configuration allows the ultimate flexibility in what test parameters are used to monitor device degradation. The voltage forcing analog circuitry consists of a high-gain, high-voltage, FET input operational amplifier followed by a power output stage. The module uses a 12-bit D/A converter to set the voltage to be forced, with 1.25mV resolution on the lowest of six voltage ranges.

In the current forcing mode, a second 12-bit D/A converter is used as the input to a voltage controlled current source (VCCS). Within the VCCS, a series of eight precision resistors correspond to the eight current ranges of the supply. This design ensures accurate current forcing from nanoamps to hundreds of milliamps.

Analog Cabling

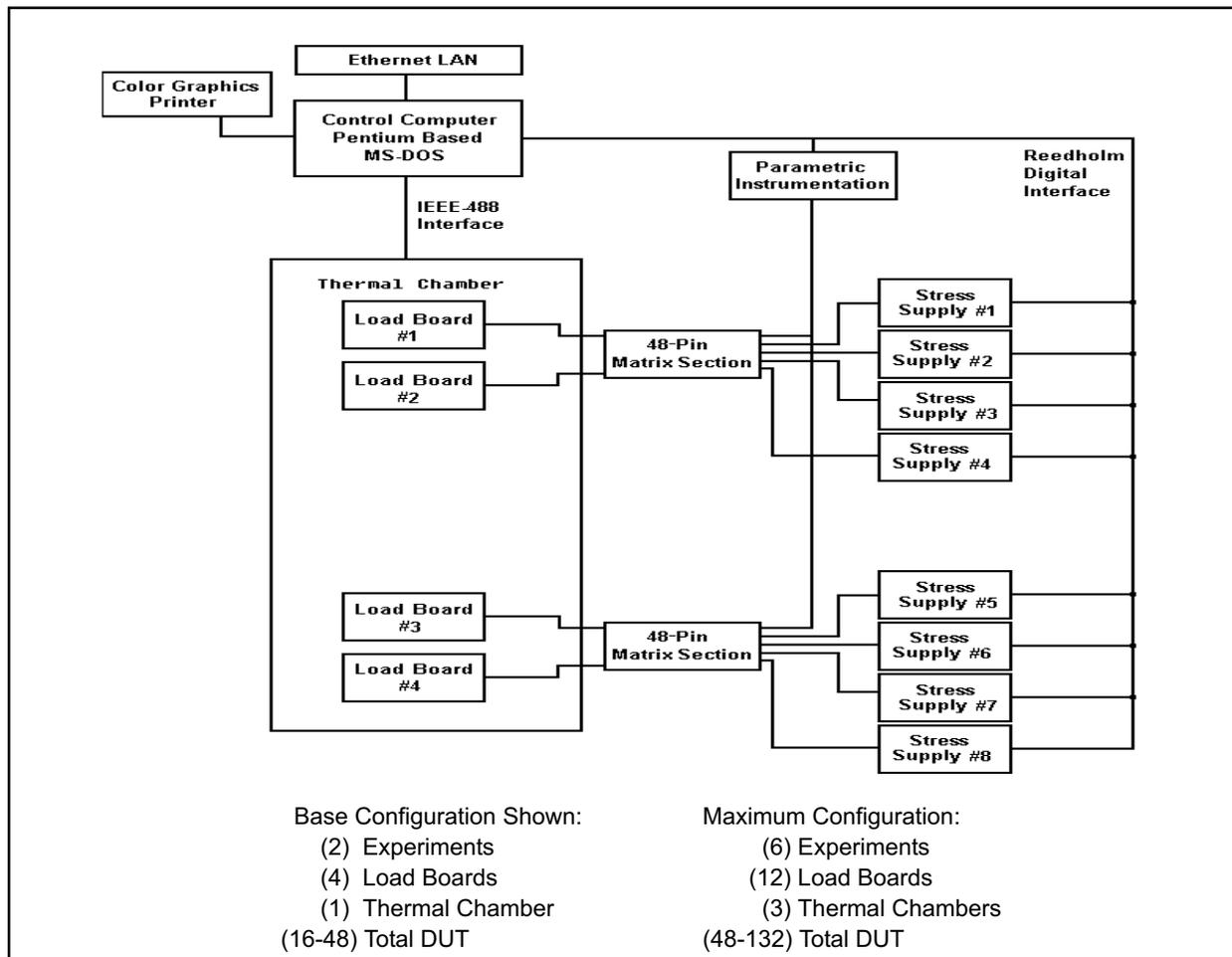
Fully guarded and shielded cabling connects the pins in the switching matrix to a rugged bracket mounted on the thermal chamber door. At both ends of the cabling, zero insertion force connectors provide quick and easy connections as well as excellent reliability. Routed through the thermal chamber's purge hole, high temperature analog cabling attaches to the load board card edge connectors.

Thermal Chambers/Load Boards

The RI-53 is delivered with the thermal chamber(s) to be used with the system. Hardware integration includes design of the internal and external mounting brackets for the analog cables and load boards, allowing for easy removal and insertion of the oven door and load boards. Normally two experiments share a single chamber, but other combinations are possible.

The load boards to be used for HCI testing are supplied. Separate load boards for TDDB testing can also be ordered. The number of devices that can be stressed on each board depends on the number of independent terminals. Finally, diagnostic load boards are provided for verification of test and measurement signals inside the chamber.

RI-53 Block Diagram



Base System Configuration

Instrument Enclosure

- Floor Standing Dimensions
- L24" x W36" x H84"
- L610mm x W914mm x H2134mm
- Static System Power Units
- (3) Backplane Assemblies
- (2) Tester Analog Cables

Tester Computer

Check with Factory for Present Model

Color Printer

Check with Factory for Present Model

Stress Instrumentation

- (8) VSM, Voltage Stress Modules

Test Instrumentation

- (1) DMM, 16-Bit Digital Multimeter Module
- (3) VFIF, Voltage/Current Forcing Modules
- (1) VF, Voltage Forcing Module

Matrix

- (12) CPM, Crosspoint Matrix Modules (96 pins)
- (1) NEM, Node Extender Module
- (2) NTM, Node Terminator Modules
- (2) 7.5' Oven Analog Cables
- (1) 9" High Temperature Analog Cable

Thermal Chamber

- (1) Sun Systems, Model EC01 (200°C)

Load Boards

- (4) Four-layer Load Boards
- (4) Diagnostic Load Boards

Handling Data

Whether experiments are in progress or complete, information about them is available in the form of logs, reports, and summaries. Figure 3 exemplifies a graphical output.

- **Logs**

A sequential log of each experiment contains dates and times of start-up, completion, and the time each scan is executed. All other status and error messages are also logged.

- **Reports**

Each report contains an experiment description, the stress conditions, and information for each scan. For every scan, the following data is shown: scan number, scan type (infant, normal, post), elapsed time, number of devices failed, percentage of devices failed, and temperature.

Reports can be displayed on the monitor or sent to the printer. They can also be sent to the hard disk for later retrieval. Reports can include data from either individual devices or all devices in an experiment. Another option allows viewing of only the infant scans, first and last normal scans, and post scans.

- **Summaries**

Summaries can be generated in two different ASCII file formats: one in report format for printing and another in PRN format for graphing via EMAGE. The summaries available include lognormal, cumulative failure, test result over time, and change in result from initial value over time.

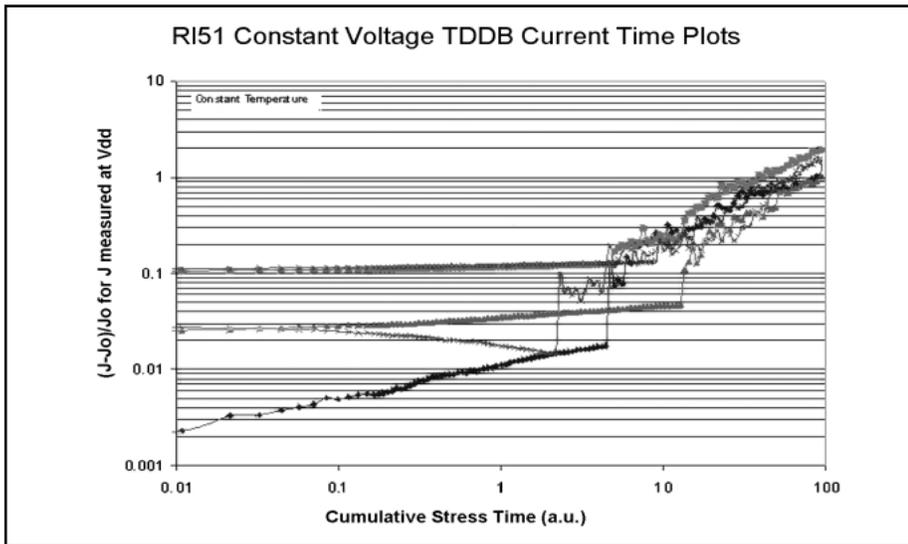


Figure 3 - Constant Voltage TDDB Results

Expected Performance

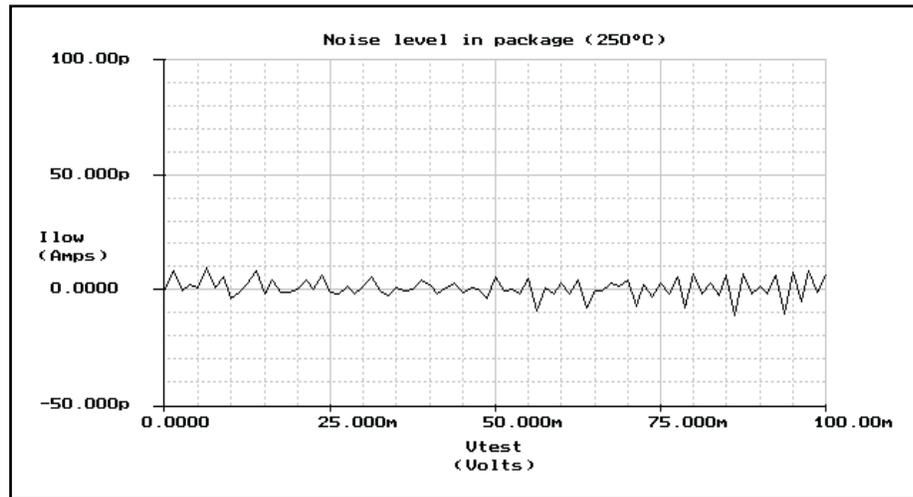


Figure 4 - System Noise, Including Load Board and Oven

Maintenance Tools

A variety of maintenance tools is delivered with an RI-53. The main system diagnostics provide an automatic method of verifying function and accuracy of system modules and cable harnesses. They also offer a self-repeating, error logging tool to detect specific problems. The diagnostic software has five major components:

- Determination of system configuration.
- Selection of modules to be tested.
- Selection of tests to be run.
- Testing for system function and accuracy.
- Creation of error and/or summary reports.

Instrument calibration is supported by a dedicated software application. Individual routines are provided for

stress supplies and measurement modules. Software control allows system calibration and repair even during active experiments.

Another program is used for real-time, analog troubleshooting of the Reedholm instrumentation. The real time debugger provides a means to connect device pins and instrumentation, to program voltages and currents, and to make measurements.

A digital troubleshooting tool allows bit level control and display of the instrumentation control registers. Additional tools provide system timing information and instrumentation checkout at the individual module level.

Support

Warranty

Each system comes with a 12-month factory warranty for defective parts and labor. Additionally, extended warranty and service contracts are available.

User Training

Training on the use of diagnostic and applications programs can occur at the factory or on site during installation. The class covers device characterization, test plan setup, experiment control, data analysis, and system maintenance.

Documentation

Complete documentation delivered with the test system includes comprehensive user's manuals describing

hardware and software along with schematics of system elements.

Application Support

Technical phone, fax, and e-mail support is available from the U.S. Monday through Friday, excluding holidays. Contact us by:

- Phone: (512) 869-1935
- FAX: (512) 869-0992
- e-mail: support@reedholm.com

Local technical support from Reedholm's distributors is also available in many parts of the world.

Specifications

Instrument hardware specifications apply at the end of a 7.5-foot analog cable without a load board attached.

Use Conditions

Temperature: 18°–28°C

Humidity: 10%–60% R.H. Non-Condensing

Nominal Power:

System—120V, 60Hz

Thermal Chamber—240V, 60Hz

Regulated supplies isolate the instrumentation from power line variations of more than $\pm 10\%$. Specify nominal voltage and frequency when different than nominal.

Switching System

A critical element of a dc reliability test system is the switching subsystem. Reedholm has taken special care to develop low-noise, high-performance switching matrix modules. Also, hazard detection software prevents “hot” switching of relays and thereby maximizes the operational life of the relays.

Maximum Standoff Voltage	$\pm 600V$
Maximum Carrying Current	$\pm 2A$
Pin-to-Pin Leakage (At 100V Guarded)	$< \pm 10pA$
Pin-to-Pin Leakage (At 100V Unguarded)	$< \pm 1nA$
Pin-to-Pin Thermal EMF	$< \pm 10\mu V$
Pin-to-Pin Resistance (Shorted)	$< 500m\Omega$
Switching Speed (Including Software Delay)	1ms

Voltage Stress Module (VSM)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Low Voltage Configuration Only				
Voltage	2.5V	2.5mV	0.05	78.125 μV
	5V	5mV	0.05	156.25 μV
	10V	10mV	0.05	312.5 μV
High Voltage Configuration Only				
Voltage	25V	25mV	0.05	781.25mV
	50V	50mV	0.05	1.5625mV
	100V	100mV	0.05	3.125mV

Notes:
 1. Accuracy of voltage forced on a given range is equal to the sum of a percentage of value forced and an offset error: value \pm (% of value error + offset error).
 For example, forcing 1V on 2.5V range:
 1V \pm (0.05% of 1V + 2.5mV)
 1V \pm 3mV

Voltage Forcing (VF) Module

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Voltage	2.5V	2.5mV	0.05	1.25mV
	5V	5mV	0.05	2.5mV
	10V	10mV	0.05	5mV
	25V	25mV	0.05	10mV
	50V	50mV	0.05	25mV
	100V	100mV	0.05	50mV

Notes:
 1. Current limit fixed at $> 200mA$.
 2. Settling time is $< 500\mu s$ to within 0.1%.

Digital Multimeter (DMM) Module

Mode	Range	Measure Error		Resolution
		Offset	% of Value	
Voltage	0.25V	250 μV (50 μV)	0.03	7.8125 μV
	0.5V	250 μV (50 μV)	0.03	15.625 μV
	1V	300 μV (75 μV)	0.03	31.25 μV
	2.5V	500 μV (100 μV)	0.03	78.125 μV
	5V	1mV (200 μV)	0.03	156.25 μV
	10V	2mV (400 μV)	0.03	312.5 μV
	25V	5mV (1mV)	0.03	781.25 μV
	50V	10mV (2mV)	0.03	1.5625mV
Current	100nA	100pA*	0.20	3.125pA
	1 μA	300pA*	0.05	31.25pA
	10 μA	2nA	0.05	312.5pA
	100 μA	20nA	0.05	3.125nA
	1mA	200nA	0.05	31.25nA
	10mA	2mA	0.05	312.5nA
	100mA	20 μA	0.05	3.125 μA
	1A	200 μA	0.10	31.25 μA

Notes:
 1. Maximum output current on 1A range is $\pm 200mA$. On other ranges, the maximum is 125% of range.
 2. Settling time to 0.01%: 4.0ms, 100nA Range
 2.3ms, 1 μA Range
 1.7ms, 10 μA -1A Ranges
 1.6ms, 250mV-100V Ranges
 3. CMRR Voltage: $< 5\mu V/V$ (106dB)
 CMRR Current: < 1 ppm of range per volt, 10 μA -1A
 < 2 ppm of range per volt, 1 μA
 < 6 ppm of range per volt, 100nA
 *4. Accuracy on the lowest three current ranges is determined with digital averaging approximating line cycle integration.
 5. Accuracy of current measured on a given range is proportional to range error and a percentage of current being measured. For example, measuring 50 μA on the 100 μA range would have uncertainty of: 50 $\mu A \pm$ (20nA + 0.05% of 50 μA) = 50 $\mu A \pm$ 45nA
 6. Range Error shown in parentheses () applies for an 8-hour period after auto-zero, and for $\pm 1^\circ C$.
 7. When measuring currents from sources with non-zero output conductance, and the following amounts to the error specification: \pm (830 ppm of value + 151pA)/mho.

Voltage/Current Forcing (VFIF) Module

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Voltage	2.5V	2.5mV	0.05	1.25mV
	5V	5mV	0.05	2.5mV
	10V	10mV	0.05	5mV
	25V	25mV	0.05	12.5mV
	50V	50mV	0.05	25mV
	100V	100mV	0.05	50mV
Current	100nA	200pA*	0.20	25pA
	1 μA	700pA*	0.15	250pA
	10 μA	5nA	0.05	2.5nA
	100 μA	50nA	0.05	25nA
	1mA	500nA	0.05	250nA
	10mA	5 μA	0.05	2.5 μA
Current	100mA	50 μA	0.05	25 μA
	1A	500 μA	0.10	250 μA

Notes:
 1. Maximum output current on 1A range is $\pm 200mA$.
 2. Settling time is $< 2.5ms$ to within 0.1%.
 3. CMRR: $< 0.002\%$ of range per output volt in current.
 *4. Accuracy is determined with digital averaging approximating line cycle integration.

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