High Voltage SMU

[HVSMU]

- **Output Voltage: Up to 250V**
- **Output Current: Up to 10mA**
- **Programmable Bipolar Voltage**
- **Independent Voltage Measurement**
- **Programmable Current Limit**
- **500V Compliance with Two Supplies**
- **Indefinite Short Circuit Protection**
- **Kelvin Sensing**
- **Access to All DUT Pins**

The high voltage source/measure unit (HVSMU) is a programmable voltage source with five programmable current limit setpoints of 1µA, 10µA, 100µA, 1mA, and 10mA. It has bipolar output capability to 250V and the capacity to measure this voltage. The analog circuitry for generating voltage consists of a precision digital to analog converter (DAC), an error amplifier, a precision voltage clamp, a voltage controlled current source (VCCS), a sense buffer amplifier, and precision feedback components.

The analog circuitry for measuring the output voltage consists of an operational voltage divider and an analog to digital converter (ADC). Referring to the block diagram of Figure 1, the voltage reference for the HVSMU is produced by a 12-bit precision DAC which outputs voltage on a full scale range of 10 volts.

The error amplifier provides sufficient gain in the control loop to ensure that its negative input will remain a virtual ground unless the load current attains the programmed limit level. Thus, for the condition of no current limit, the output voltage is determined by the ratio R_2/R_1. Since this ratio is equal to 25, the output voltage range is 250V.

The voltage clamp prevents the VCCS input from exceeding a magnitude of 5 volts. Therefore, the maximum output current is proportional to the 5 volt input level.

Within the VCCS is a selection of five precision resistors which correspond to the five current limit setpoints and determine the transconductance of the VCCS. The output current maximum is determined by the product of the 5 volt clamp level and the VCCS transconductance.

The sense buffer ensures that the output voltage is not affected by any voltage which may be dropped down the force line. Because no current flows down the sense line, the sense buffer ensures that all of the VCCS output current flows to the DUT load.

Specifications ($18°C \leq T_A \leq 28°C$)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Voltage Source	250V	250mV	0.1	125mV
Voltage Monitor	250V	250mV	0.2	125mV
Current Limit	1µA	N/A	0.2+0.004/Vout	N/A
	10µA-10mA	N/A	0.1+0.004/Vout	N/A

Comments:

1. Drives the signal shield in Current or Voltage mode.
2. Output voltage can be independently measured with the on board A/D converter.
3. Current limit selectable in decade steps from 1µA to 10mA.
4. Accuracy of voltage forced is proportional to the range offset error and a percentage of value forced. For example, forcing 100V on the 250V range:
   100V ± (250mV + 0.1% of 100V)
   100V ± 350mV
5. Accuracy of the current limit is proportional to the limit value and the actual output voltage of the limit point. For example, 1mA at 100V:
   1mA ± (0.1% + 0.004%/Volt x 100V) of 1mA
   1mA ± 0.5% of 1mA
   1mA ± 5µA

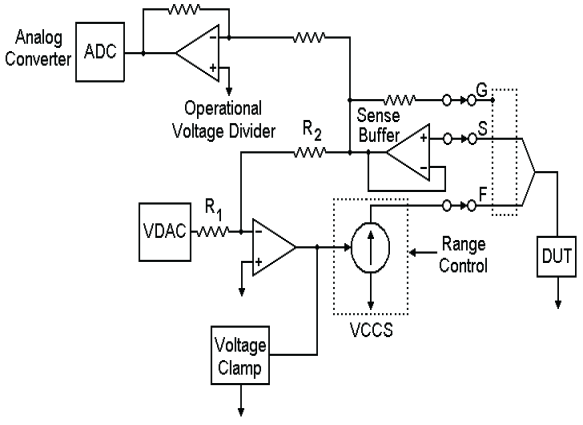

Figure 1 - HVSMU Block Diagram

The operational voltage divider serves to reduce the output voltage to be measured by the ratio of 25:1 so that the voltage is scaled properly for the ADC; of which full scale input is 10V in magnitude. Finally, the HVSMU is connected to any of the five analog nodes on the backplane via a three pole switch that allows the accuracy enhancing feature of Kelvin sensing within a fully encompassing guard shield.

Although the HVSMU can supply up to 10mA to a load, the HVSMU is fully protected against output short circuits, even when shorted to the output of another HVSMU. During such a condition, heat dissipaters on the output stage transistors are sufficient to allow the short to continue indefinitely.

The HVSMU output step response is heavily dependent upon the current limit setpoint and the magnitude of the step change. Because this is a high voltage unit, its step response time is dominated by slew rate limiting in the control loop. These effects are shown in Figures 2-6 for various step levels.

Normalized Step Response

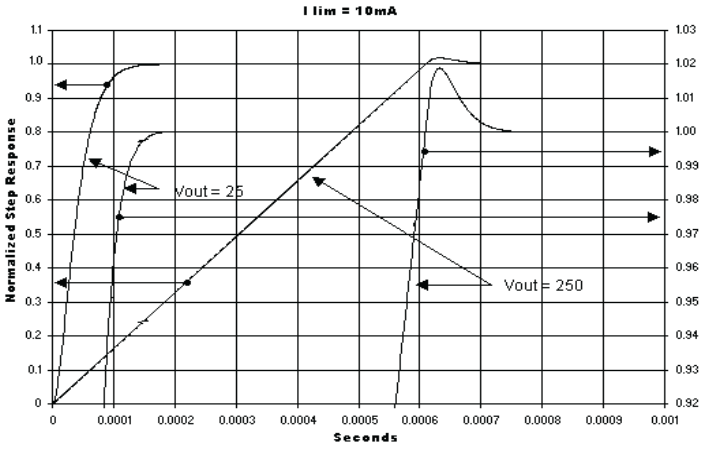

Figure 2 - I_{LIM} = 10mA

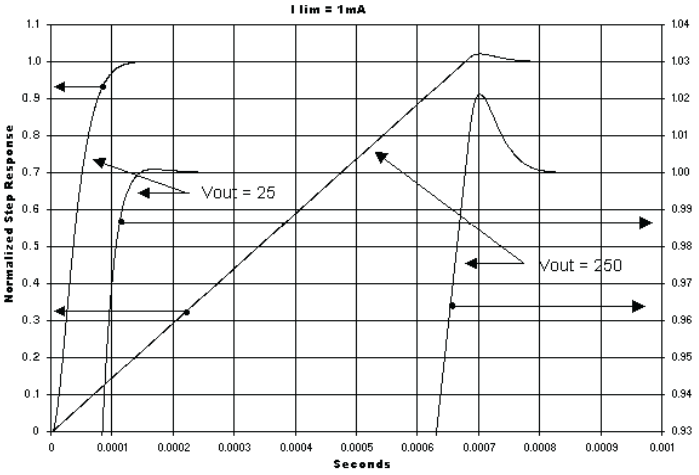

Figure 3 - I_{LIM} = 1mA

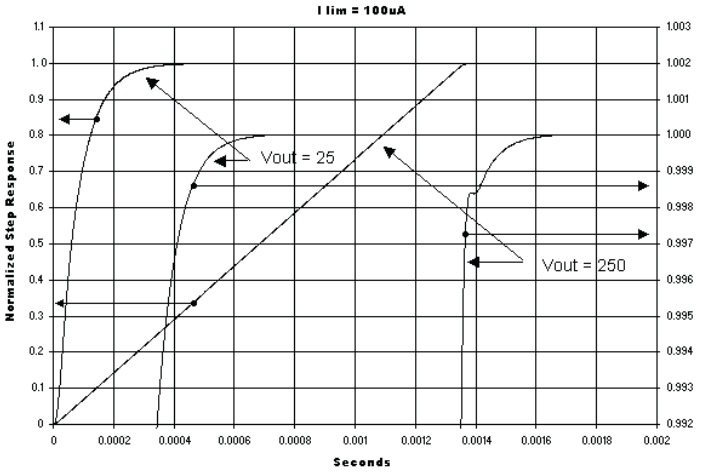

Figure 4 - I_{LIM} = 100µA

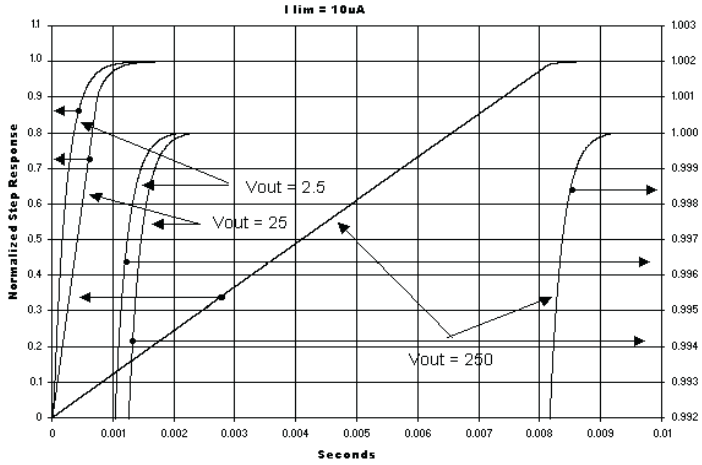

Figure - 5 I_{LIM} =10µA

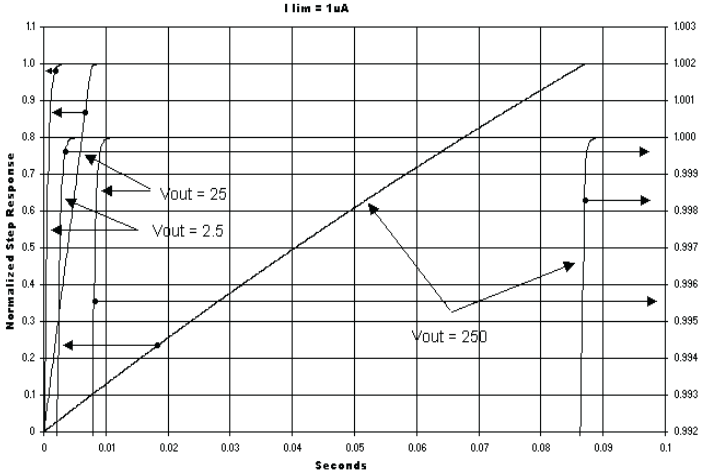

Figure 6 - I_{LIM} = 1μA