APPLICATION NOTE

AN-117

Using VFIF's for Bias Current Measurements

Overview

For complex devices that cannot be quickly powered on and off, and that need bias current measurements at several ports, a procedure has been developed for using VFIF's to make current measurements. These procedures are part of optional CCD test code that can be applied to Reedholm parametric test systems as well as the high pin count RI-70 system.

Software-based current measurements address those few instances in which the Reedholm VFIF/DMM combination is not readily configured to provide superior testing control when compared with an SMU instrument architecture. This report provides some background on those two approaches in addition to describing the software-based measurement.

VFIF and DMM Combination

VFIF and DMM are acronyms for **V**oltage **F**orcing, Current (**I**) **F**orcing supply and **D**igital **M**ulti-**M**eter. These modules provide measurement combinations of:

- Forcing voltage and measuring current
- Forcing voltage and measuring voltage
- Forcing current and measuring current
- Forcing current and measuring voltage

Figure 1 illustrates a simple test condition with a VFIF outputting V_{test} to a resistor and a DMM making a current measurement. Remote, or Kelvin, sensing is provided to the device under test, thereby making sure that the test voltage is delivered to R_{DUT} plus the incidental connection/fixture resistances R_{dh} and R_{dl}. Wiring resistances R_{fh}, R_{sh}, R_{fl}, and R_{sl} are not factors because zero current in the voltage sensing paths ensures that V_{test} is delivered to one leg of the device under test and analog ground (0V) is delivered to the other.

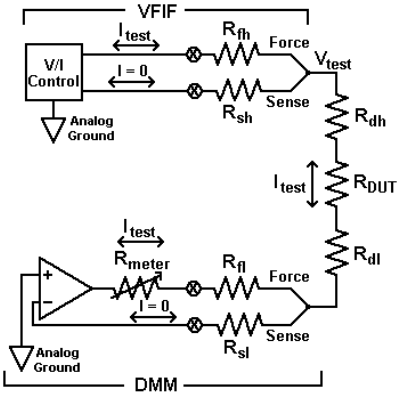

Figure 1 – VFIF/DMM Force V, Measure I

Each of the four measurement combinations is more effectively done with a VFIF-DMM pair than with a single SMU. In fact, to get the full benefits of the VFIF-DMM combination requires two SMU's.

SMU Implementation

Contrast the SMU implementation in figure 2 with that of figure 1. The first problem is that R_{fl} and R_{sl} play a significant part in measurement accuracy for low resistance values. Another problem is that the current sensing amplifier is biased at the common mode potential, V_{test}, thereby converting a portion of V_{test} to a current measurement error. Thirdly, there is a single point of control for current. If the current range of the metering amplifier is too great, damaging device current can flow. Yet, if the current range is too low, it will take a long time to charge parasitic capacitance. Effects of R_{fl} and R_{sl} can be addressed at the cost of using a second SMU to provide Kelvin sensing.

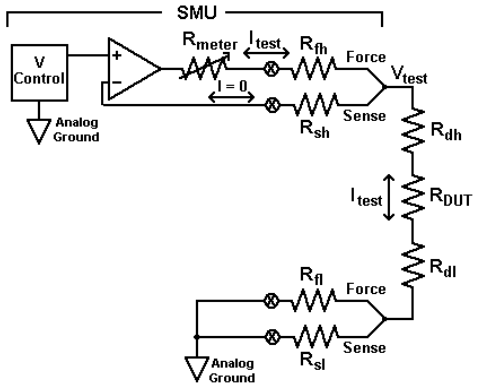

Figure 2 – SMU Force V, Measure I

Parametric Testing

When applied to dc parametric testing, forcing voltage on one device leg and measuring current on another is typically the fastest, most accurate way to make semiconductor device measurements. Furthermore, there is usually a single device measurement per test, even if several power supplies provide bias to the device under test (DUT). As noted, designs that combine sourcing and measurement functions into a source-measurement unit (SMU) compromise performance of each function. Those are some reasons why Reedholm provides four current/voltage crossover sources (VFIF's) and a digital measurement module (DMM) in the basic system instead of SMU's.

That is not to say that Reedholm does not supply SMU's. However, the ones that are supplied are needed for very high voltage and very high currents. Because of that focus, performance limitations of SMU's are restricted to those few measurements requiring special capabilities.

Multiple Measurements Made Quickly

When multiple measurements need to be made on simple devices that require multiple biases, Reedholm algorithms, switching speeds, and power up/down methods permit taking several measurements in the same time frame achieved in SMU based systems.

Functional CCD Testing

Functional device testing sometimes requires multiple biases and multiple measurements. Unfortunately, latch-up considerations require careful power up and down sequences that are difficult to do rapidly.

Figure 3 illustrates a requirement to power an area CCD device, connect input/output pins (or leave them floating), and determine bias currents from five supplies. In this case, V_{dd} current could be as much as 2A, so an IEEE-488 controlled power supply with current read back was used. It was connected through a user function interface to one of the five active system nodes. The other four nodes were biased with VFIF's and connected to the lower bias current CCD power supply input pins. Multiple pins were tied together at each supply input.

CCD Testing Code

CCD testing is a simple extension of Reedholm dc parametric testing, but organization of test plans for productive use is quite different. Instead of many test types, CCD testing only requires a few. On the other hand, CCD test plans are quite large since there is a great deal of repetitive testing with the same conditions and limits for each test. Assigning pin and test conditions for each test would be quite laborious had pattern-based software not been developed that automates pin assignments, and generates pattern-based reports.

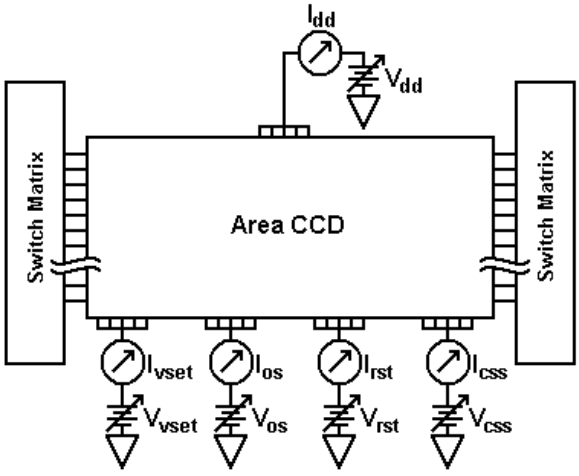

Figure 3 – CCD Connections for Bias Measurements

RDS Intranet Availability

Reedholm CCD test code is an option available for RDS Intranet users. It can be installed on Reedholm parametric test systems as well as the high pin count RI-70 systems.

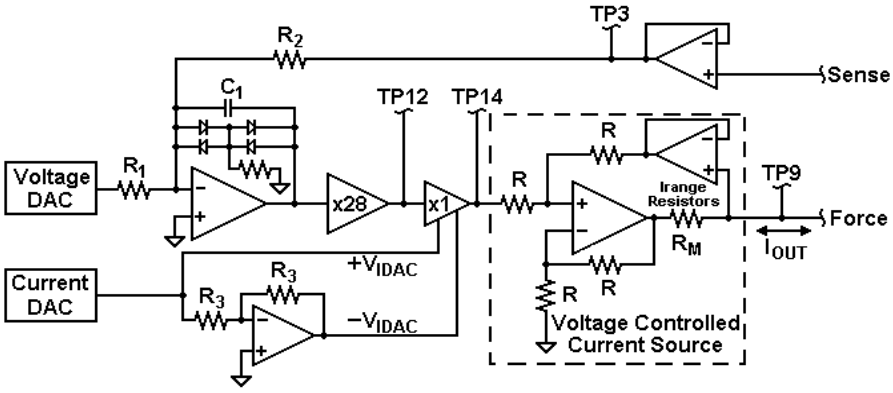

Figure 4 - VFIF Block Diagram

VFIF Operation

To explain operation of the bias current code, some background on VFIF operation is needed. Figure 4 is a simplified VFIF block diagram showing independently controlled voltage and current D/A converters (DAC's). In voltage mode, output current is adequate to drive the VFIF load and produce current through R_2 that cancels that through R_1 and thus balances the feedback loop. Current mode occurs when output current is too small to drive the VFIF load and keep the feedback loop closed. While in current mode, output current is precisely controlled by voltage from the current DAC.

Voltage Mode Control

The voltage DAC has three base ranges: ±2.5, ±5, and ±10V full-scale. Output voltage delivered to TP3 is governed by the feedback ratio $-R_2/R_1$. When R_1 is equal to R_2, output voltage is the inverse of the voltage DAC output. If R_1 is reduced by 10:1, output voltage is amplified by x10 to provide full-scale outputs of ±25, ±50, and ±100V. The voltage controlled current source acts as a high gain voltage amplifier whose current output is determined by the voltage at TP14. As long as the buffer output is not clamped (i.e., $<|V_{IDAC}|$), feedback adjusts the buffer output to whatever is required to drive the VFIF load.

Current Mode Control

Output voltage from the current DAC, and its complement, are the supply voltages for a N/PFET follower shown as a buffer amplifier. When the amplifier input is too great, the buffer clamps at $+V_{IDAC}$ or $-V_{IDAC}$ and thus opens the voltage feedback loop. Clamping limits output current to $|V_{IDAC}|/R_M$ through action of the output amplifier. As there are eight current range resistors (5 to 50MΩ), and as the maximum V_{IDAC} is 5V, current ranges are ±100nA, ±1µA, ±10µA, ±100µA, ±1mA, ±10mA, ±100mA, and ±1A. The standard VFIF output is limited to ±200mA on the 1A range.

Current Limit Detection

Current limit mode is detected with level comparators connected to the input of the buffer amplifier (TP12) and set to ±10.5V, regardless of V_{IDAC} level. The VFIF goes into current mode when the signal at TP12 is $|V_{IDAC+}V_{TH}|$ where V_{TH} is the threshold voltage for the N or P channel JFET. For V_{TH} ~2V, the voltage at TP12 has to change another 3.5V to effect a limit bit change when current is set to 100% of range, or V_{IDAC}=5V. When current is set to 1% of range, V_{IDAC} is 50mV, and the change at TP12 has to be ~8V for a limit bit change.

Voltage to Current Mode Transition

As VFIF output voltage is linearly ramped to force a transition between voltage and current mode, there is no discontinuity as the output current clamps exactly at the set point. However, the current limit comparator is not triggered at that point, and won't be until the voltage at TP12 reaches ±10.5V. In fact, if the output voltage is held slightly above the transition point, the current limit bit will take a very long time until the voltage at TP12 is high enough.

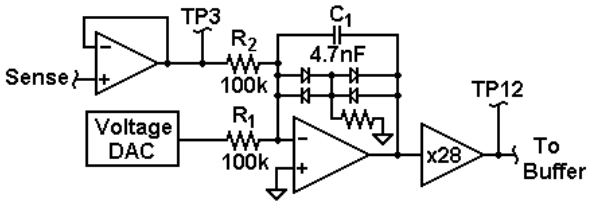

Figure 5 – Voltage to Current Charging Circuit

Referring to figure 5, assuming a current setting equal to 100% of range, voltage at TP12 will be ≅|7V| immediately prior to the current mode transition. That would require ~250mV at the input to the x28 amplifier. Thus, there would be almost no current through the diodes and C_1 would be charged to 250mV. Current R_2 would match that through R_1, albeit in the opposite direction.

If the voltage DAC generates a stepped voltage ramp, the effect will be a square function increase to 10.5V after the conversion from voltage to current mode. Figure 6 shows the timing relationships starting with the VFIF output (V_{OUT}) reaching clamp and eventually causing the current limit bit to change state. R_{OUT} is the load resistance at the output of the VFIF.

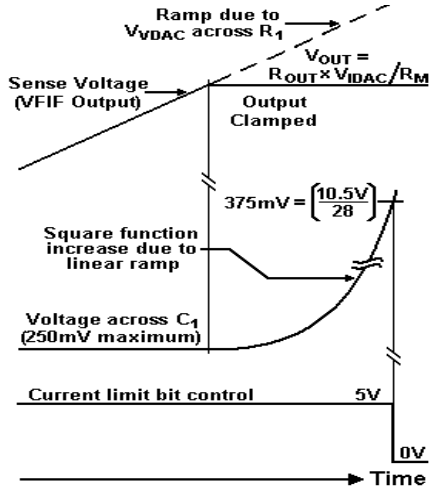

Figure 6 – Events Causing Current Limit Bit Change

Time to Reach Current Limit

Figure 6 is a qualitative illustration of the delay between going into current mode and triggering of the limit bit. To get a quantitative feeling for what delays might be, the ramp could be stopped as soon as current mode is reached, step voltages could be applied from the voltage DAC, and time to reach 375mV (starting from 250mV) determined for each step. Predicted results are shown in table 1 based on the first order capacitive displacement current equation:

$$\Delta T = C_1 \times \Delta V/(Vstep/I) \text{ where:}$$
$$C_1 = 4.7nF$$
$$\Delta V = (375\text{-}250)mV, \text{ and}$$
$$I = Vstep/100k\Omega$$

Voltage Step (mV)	Δ Time (msec)
1	58.8
5	11.8
10	5.88
50	1.18
100	0.588

Table 1 - Current Limit Bit Delay

While the table is for steps in the voltage DAC, charging of C_1 determines response time, and the current DAC would be the driving source while in current mode. Since R_2 is the same value as R_1, delay times are the same if the current DAC caused the same output voltage steps.

Limit Bit for A/D Conversion

As noted in figure 6 for a load, R_{OUT}, VFIF output voltage is proportional to the current DAC voltage, and the ratio of the load resistance divided by the range resistor. Thus, adjusting V_{IDAC} and monitoring the current limit bit can yield the precise current at which VFIF operation switches from voltage to current mode.

Linear Sweep Too Slow

Given the data in table 1, the sweep must be very slow for good resolution. For instance, with a load resistance equal to the range resistor, a V_{IDAC} change of 5mV, or 0.1% of range, would take 18.3msec to register. And a linear sweep across the full range would take 18.3 seconds. Those kinds of times are not feasible. If they were, it would be faster to power the IEEE-488 supply down and up four times to get the four bias currents required for CCD applications.

A resolution requirement of 1% would reduce linear sweep time by 10:1, but that is still much too slow.

Binary Search Faster, But Still Slow

Figure 7 illustrates VFIF output voltage while the current DAC is ramped from 0 to full scale. Transition from current to voltage mode happens slightly above 50%. When the DAC is at 0V, no output current flows, so the output voltage is zero. As V_{IDAC} increases, output voltage follows R_{OUT}, and the VFIF stays in current mode until the VFIF set voltage is reached. Then the VFIF goes into voltage mode. In a binary search with 0 and 100% endpoints, the first comparison is at 50%.

- If the current limit detector output were still true, indicating current mode, the next step would be at 75%, halfway between 50 and 100.
- If not true, indicating voltage mode, the next step would be 25%, halfway between 50 and 0.

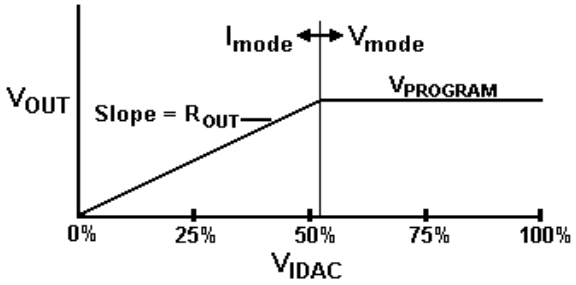

Figure 7 – Binary Search Decisions

Subsequent tries would split the difference, with the limit bit determining which direction the next step would take. It would take ten such steps ($2^{10} = 1024$) for 0.1% resolution (1 part in 1024). For 1% resolution, seven steps would be needed ($2^7 = 128$).

For simple binary searches, a detection error sends the algorithm in the wrong direction from which there is no recovery. In the illustration above, if the 50% decision were wrong, the next try would be at 25%, and each succeeding one would get closer to 50%, but never reach it. That is the reason delays have to be long enough to accommodate the full desired resolution. Thus, for 0.1% resolution, one would have to wait 18.3msec at each step, or 183msec for a full search. For 1% resolution, steps would be 1.83msec, or 18.3msec for the search.

Bias Current Measurement Requirements

- Unlike device current measurements, bias current measurements on good devices can span several decades, so the search code needs to automatically range, starting with the maximum current that the user input.
- Speed needs to be fast without sacrificing much resolution. That was met with maximum measurement time per range of 12msec.
- Voltage perturbation needed to be less than a diode drop to prevent inadvertent forward biasing of substrate and diffusion regions.

VFIF Bias Current Measurement

Using a linear ramp is too slow if one waits for the limit bit to be accurate for each step. But it is possible to use a much faster ramp and interpolate the current causing transition from voltage to current mode.

Two Fast Ramps

The first plot in figure 8 shows the sequential, high-speed current DAC ramps used to extrapolate bias current. Starting at 5V (or 10mA), the first ramp decreases until the limit bit changes state (becomes true), then the second ramp increases until the limit bit becomes false. Bias current is then interpolated by averaging current DAC values at the end of each ramp.

Besides illustrating software operation, low voltage bias (650mV) that produced 6.5mA into a 100Ω load shows that output voltage perturbation is quite small. Since 10mA was the starting range, no range change was needed.

The spike on TP3 occurred after the VFIF had been disconnected from matrix, so it did not reach the device. Also, device pins are grounded after a test, further assuring that no damaging voltages reach the device during power down.

Ramp Speed

Both ramps are decremented or incremented by 0.1%, or four least significant bits (lsb's) per step. For each step, a few comparisons, simple calculations, and two instrument calls (AMPS and PSLIMIT) are performed. From figure 8, the first ramp dropped from 5V to ~3V in 7.5msec. Since 5V represents 1000 steps, a 2V drop takes ~400 steps, so each step took ~19µsec, which is consistent with the time those calls take.

Voltage to Current Mode Transition

When the second plot in figure 8 starts down from 650mV, the VFIF has transitioned from voltage to current mode even though current limiting is not detected for ~2msec. Calculations in table 1 are consistent with

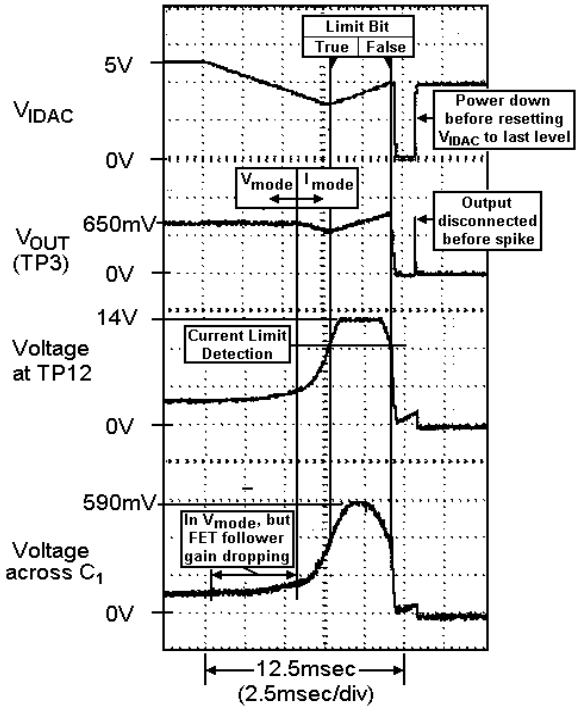

Figure 8 – Waveforms for 10mA Start Current, 650mV Bias, and 100Ω Load

timing in figure 8. That is, output voltage starts down, and manages to decrease by 150mV, around 2msec before current limit is detected.

Current Mode Ramp

As the transition to current mode happens far before the current DAC voltage ramp is started, and since the limit bit detection is used to end both ramps, the VFIF is in current mode for the entire second ramp even though the limit bit turns off.

Figure 9 shows the signal path from the current DAC output to TP12 where the limit condition is detected. To simplify explanation, force and sense were shorted, the FET follower was removed, a single polarity of V_{IDAC} used, and the voltage DAC was removed.

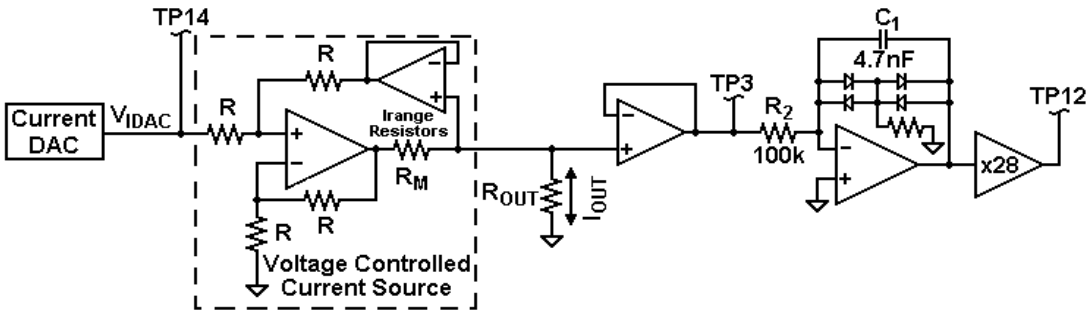

Figure 9 – Signal Path for Current Mode Limit Bit Triggering

Integrator Response

Referring to figure 8, current limit detection is at TP12, but the signal has been clipped at that point, so it is not convenient for showing integrator behavior. However, the voltage across C_1 is well behaved, so it is used along with the output voltage at TP3 to illustrate how the integrator is used to determine bias current. Waveforms from figure 8 were also cleaned up for the illustration in figure 10.

I_{OUT}, or V_{OUT}/R_{OUT}, is the actual bias current that needs to be determined. In figure 10, the three current-time pairs (I_1,T_1; I_2,T_2; I_3,T_3) represent currents flowing at precisely those points in time. Voltages V_1 and V_2 are associated with the current-time pairs as shown. There is no third voltage because it is the same as V_2. Time T' is when the second ramp is equal to I_1, the desired current. Unfortunately, there is no direct way to measure it except by waiting indefinitely. However, the linear ramp to I_2:T_2 puts the VFIF in a state from which a geometric solution is apparent.

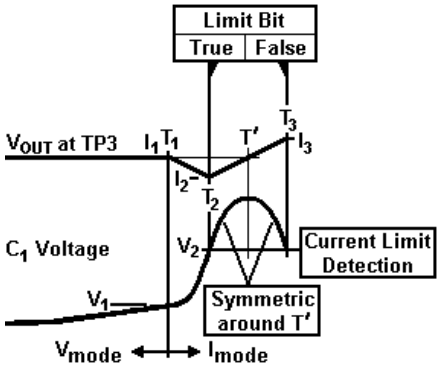

Figure 10 – Integrator Relationships

From T_2 to T'

Although the current DAC ramp goes positive after T_2, voltage across C_1 continues to increase until the ramp current is equal to I_1. At that time (T'), currents through R_1 and R_2 are in balance, so voltage across C_1 is constant, and at a peak.

From T' to T_3

After peaking at T', the output ramp continues to increase, but now charging current is in the opposite direction since current through R_2 is now greater than that through R_1.

Because the integrator voltage-current relationship is invariant and has no hysteresis, and because the current ramp is linear, voltage across C_1 decreases in a manner that its voltage-time plot is rotationally symmetric around T'.

Determining I_1

As a result of symmetry,

$$T_3 - T' = T' - T_2, \text{ which leads to:}$$
$$I_1 - I_2 = I_3 - I_1 \text{ and}$$
$$I_1 = (I_2 + I_3)/2$$

Startup and Autoranging

An autoranging scheme was implemented because predicting bias current is not always possible even though doing so maximizes test throughput.

The starting condition for bias current measurement is with the VFIF at the maximum current setting. After a three-millisecond delay, the limit bit is checked. If the VFIF is in current limit, the test is halted and an error message generated.

Assuming that the VFIF is not in limit, the first ramp described above is started. That is, the current DAC is decremented by 0.1% in a tight loop until the current limit bit goes true after which the positive ramp is used to measure current.

Downranging

If the limit bit is not true by the end of the decrementing ramp (defined as 5% of range), the next lower range is selected unless already on the 100nA range. A ramp with 1% steps (or 10x faster) is used to set the output of the new range. Ranging continues until the 100nA range is reached at which time bias current is measured. Figure 11 is an example of starting on the 100mA range with 95V bias and 100kΩ load. Note that 0.95mA was provided on the 10mA range.

Validating New Range

Before restarting the next down ramp, the limit bit is checked after a three-millisecond delay. This assures that the new range can provide the current. If the VFIF is in current limit, the previous range is restored, autoranging is disabled, and bias current is measured.

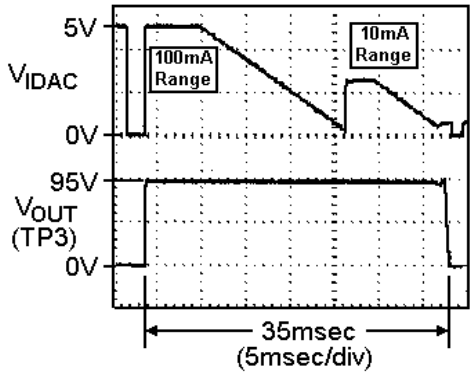

Figure 11 – Single Range Change & <10% of Range

Other Autoranging Examples

Figures 12 and 13 show two starting conditions (100mA and 200mA) for the same test conditions: 5V bias with a 100kΩ load resulting in ~50µA current.

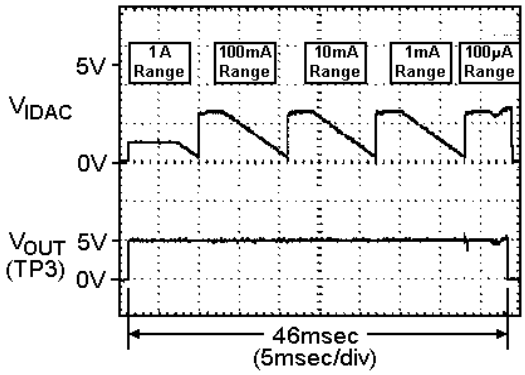

Figure 12 – 200mA Starting Condition

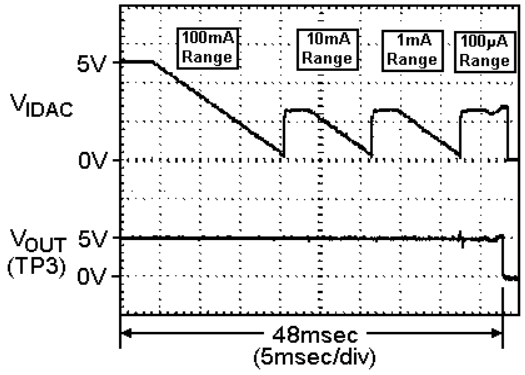

Figure 13 – 100mA Starting Condition

Measurement Performance

Table 2 shows differences between the bias current routine results and those taken with the EMPAC current at a voltage algorithm. In both tests, a VF was biased at 0V in the return path to minimize effects of ground resistance. R_{OUT} resistors were 0.25W, 5% carbon film. Starting bias currents were 200mA.

ROUT (Ω)	Difference (% at 5V)	I_{OUT} w/EMPAC
100	0.15	50.26mA
1k	0.23	5.025mA
10k	0.18	503.0µA
100k	0.56	47.7µA
1M	1.0	5.00µA

Table 2 - Measurement Differences

Uncertainty Estimate

Since ramp steps are 0.1% of range, uncertainty is one-half of the step, or 0.05%, at the start and end of the final ramp. As those uncertainties can be in opposite directions and thus add to one another, total uncertainty is 0.1% of range.

Values for the first three currents in table 2 were approximately 50% of range, so the predicted total uncertainty expressed as a percentage of value would have been 0.2%. Thus, differences were consistent with the uncertainty calculation.

For the last two ranges, the final range was not reached, so the uncertainty would have been 10x higher, or 2%. Thus, those differences are in line.

In comparing results, VFIF voltage uncertainty is not a factor in comparing the two measurement approaches. That is because PS#1 was used in both approaches. However, VFIF current sourcing uncertainty and DMM current measurement uncertainty could contribute to the differences.

In conclusion, measurement uncertainty of the bias current routine adds ~0.1% of range to that of the VFIF-12.

Addenda - Reducing Transients

When output voltages are significantly higher than the current output DAC, the effective R_{OUT} (figure 9) in conjunction with the metering resistor R_M acts to amplify V_{IDAC} when the VFIF goes into, and out of, current limit. As a result, a few tens of mV change in V_{IDAC} resulted in >2V increase when V_{OUT} was 20V. That level of change is consistent with the transients shown in various figures (8, 11, 12, and 13), but was too large for CCD applications.

The transient is due to lack of instantaneous response of the VFIF limit detection, so it was necessary to reduce ramp speed in order to reduce transient size. In addition, changes were made to handle power down after the test so that a current limit condition would not cause overshoot when decreasing to 0V.

Achieving Overshoot <500mV

Slightly less than one diode drop was selected as acceptable overshoot, regardless of level. To assure that with an output voltage of 5V, the V_{IDAC} ramp rate was reduced by 4:1 from 0.1%/step to 0.025%/step.

Overshoot at 5V of 500mV resulted in 2V overshoot at 20V, so the rate had to be reduced further for output voltages >5V. That was done by decreasing step size based on a linear equation with step size being inversely proportional to output voltage.

For a VFIF-12, the starting step of 0.025% corresponds to one lsb, so it sometimes takes multiple loops to accumulate a change of one lsb. That is not a problem in reducing ramp rate because the loop for checking current limit does not change from 19µsec/step.

Results

Figures 14 through 16 on the right show the results when an output of 20V.

1) Peak-to-peak voltage of ~0.5V in figure 14 is barely discernible unless the sensitivity is dramatically increased.
2) Current can be measured in ~160msec if the starting range (figure 15) is the right one.
3) Autoranging through four range changes to the 10µA range does not take four times as long because subsequent ramps start at 50% of scale.

Conclusions

While changes made for CCD testing did slow up testing, this test is typically run once per device, so overall test throughput is not significantly affected, and picking the right starting range mitigates the effect.

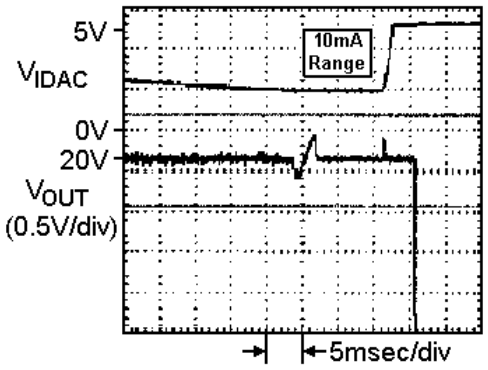

Figure 14 - Transient with 6kΩ Load at 20V

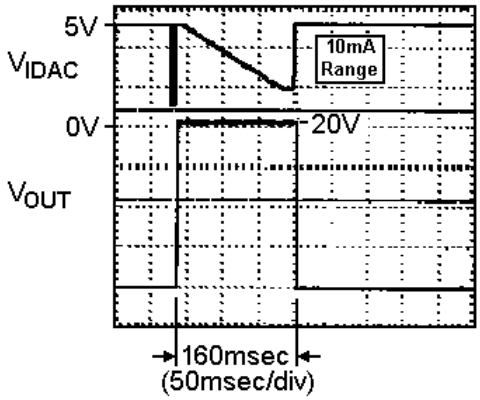

Figure 15 – No Ranging for 6kΩ Load & 10mA Start

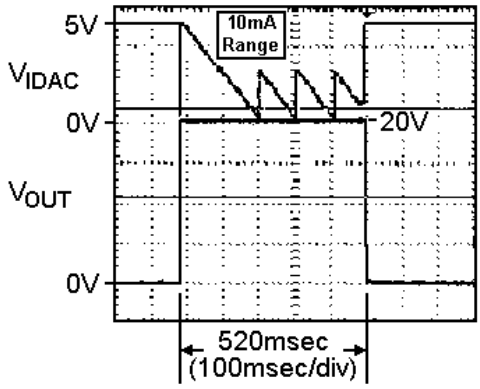

Figure 16 – Autoranging w/10MΩ Load & 10mA Start

The alternative of using an autoranging meter or SMU would be faster, but would be apt to introduce transients at range points as large, or larger, than 2V. So using this technique appears to be a sound long-term solution for CCD applications.