APPLICATION NOTE

AN-125

Measuring R_{DSon} and V_{CEsat} in Biased Chuck Systems

Overview

High power devices built on silicon carbide and other types of substrates achieve maximum performance through use of vertical structures with the drain or collector at the bottom of the stack. The RI-2kV/5A and RI-7kV/5A dc test systems contact the wafer backside, and thus the bottom of the stack, through Kelvin sensing leads capable of delivering ±5A at voltages useful for saturation measurements, or at +2kV to +7kV at currents useful for breakdown measurements. Footprint of the system is minimized by installing instrumentation in the base of a low cost, high-speed prober. Since catastrophic transistor breakdown generates large amounts of radiated and conducted EMI, the prober and test system have to be modified to ignore and/or recover gracefully from device breakdowns.

Screening high power transistors also requires measurement of low level on resistance and saturation voltage. That is the subject of this note.

Turn-on Parameters

In accordance with JEDEC standards, the baseline value for R_{DSon} is at zero power dissipation. Since the junction should be at 25°C, an infinite heat sink is implied with the chuck at room temperature. Making the measurement with short pulses, or at low power, prevents heating and allows it to be made on an automatic prober. This is important since R_{DSon} has a positive temperature coefficient that results in large shifts with modest heating.

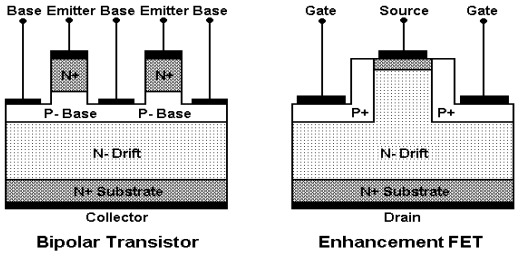


Figure 1 - Vertical Transistors

Low Power R_{DSon} Measurements

Most field effect devices do not have a separate current dependent voltage term in saturation, so if the channel voltage can be measured accurately, low currents can be used to determine R_{DSon}. An RDS DOS or Intranet force current, measure voltage test type can be used to measure on resistance of a few milliohms. In setting up for this investigation, a short length of bus wire was first measured on a bench DMM at 23mΩ. But even precision DMM's have a difficult time measuring low resistance, so resolution was lower than possible with Reedholm systems. The following page covers setting up these types of measurements.

Variability at 100mA

Forcing 100mA into 23mΩ produces 2.3mV, which is well above the 20μV shot noise of DMM-16 input stage amplifiers. So taking 100 resistance readings produced an average of 21.35mΩ with peak-to-peak variability <1%. For that sensitivity, line synchronous averaging was used, so each reading took 25msec. Heating was insignificant because only 2.135mW was dissipated during the measurement. By increasing current to 200mA, R_{DSon} as low as 500μΩ measurements would be repeatable to <5%, or <25μΩ. If there is mobility degradation at higher currents, the HISMU needs to be used.

High Current, Low Voltage Testing

Forcing voltage and measuring current works well for fairly large dynamic resistance, but is not suitable when resistance is much below 100mΩ. That is because bandwidth reduction at very low resistance prevents current from reaching its full value before the end of the Reedholm HISMU voltage pulse.

Fortunately, getting down to the low levels of R_{DSon} is possible with a pulsed voltage SMU if a stable resistance is placed in series with the drain or collector. A precision, zero TCR resistor is not needed since the test system can make a precise measurement of the resistance for automatic compensation.

Cabling for Chuck Bias Options

Before describing test connections for measuring very low channel resistance and saturation voltages, it might help to review analog cabling up to the probe card shown in figure 2.

A tester and/or prober analog cable (TAC/PAC) brings seven matrix and eight HISMU Kelvin sensed connections to a 48-pin card edge connector. Matrix pin positions 8 to 24 are unpopulated. For higher pin count applications, two matrix modules can be added along with 16 twin-axial cables.

HISMU pins for currents 0 to ±5A are wired to card edge pins 25 through 48 with two force and one sense connection per HISMU pin. Thus, one HISMU pin can have two probe needles to carry high current and one needle to sense voltage on the wafer. Matrix pin paths can be jumpered on the card to permit continuity checking between needles that are intended to share current.

Care is taken to minimize voltage drop at high currents. Along with the HISMU return wire that delivers

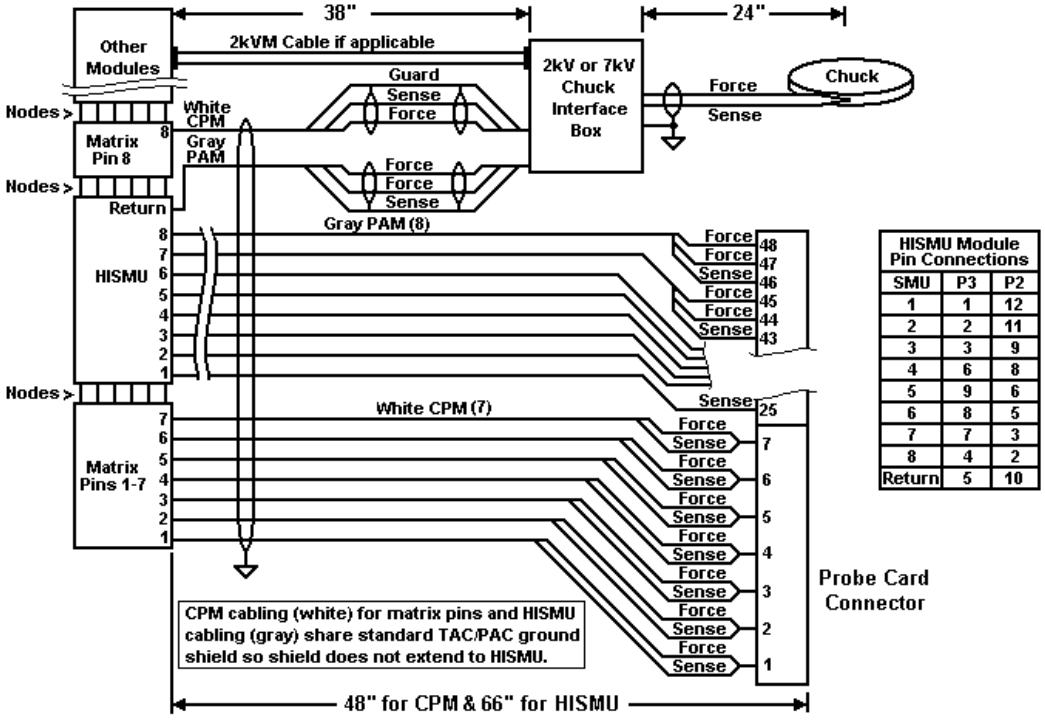


Figure 2 – Prober Analog Cable Diagram

This scheme allows single probe needles for each matrix pin path. Those connect to instrumentation capable of ±100V and ±550mA as well as the HISMU at ±2A through the matrix. In most cases, matrix pin paths are used for base or gate connections. Also, matrix pins are used as return paths for HV breakdown tests.

drain or collector current, twisted pairs of #24 wire share the emitter or source currents. Sensing is done with the shield of each HISMU cable. Five and a half feet of twisted pair wire at 13Ω/1000ft produces 72mΩ per cable. There could be 20mΩ through the card edge connector and probe card before the probe pins. Thus, Kelvin sensing compensates ~92mΩ per HISMU pin. Return path resistance is higher at ~200mΩ due to relay switches and printed circuit traces in the chuck box, but does not affect drive voltage.

Probe Card Connections

Figure 3 depicts probe card connections for the full range of tests possible with the RI-2kV/7kV 5A test systems. In addition, VFIF and DMM resources are depicted for low voltage measurements of field effect FET (R_{DSon}) or bipolar (V_{CEsat}) transistors.

Five CPM pins are referenced in this note: four are shown connected on the card, and pin 8 is connected through the chuck box as is the return input for the High Current SMU. Sense and force connections are brought through the chuck box to provide Kelvin sensing at the chuck so that 0V can be held at the drain/collector while the source/emitter is biased negatively for an N-channel or NPN transistor. Biasing of the gate/base needs to take source/emitter biasing into account.

The DMM is shown connected for differential voltage measurements, but that does not mean there are any restrictions on making current measurements.

Two HISMU input pins are shown, both of which independently sink or source up to |5A|. In this implementation, the chuck is always referenced to system analog ground, and the high input is referenced to the voltage pulse generated within the HISMU. Internal to the HISMU, higher voltages are generated as necessary to output the programmed pulse and hold the chuck at 0V. So that ±10V compliance voltages of the HISMU amplifiers do not cause amplifier saturation, probe to pad contact resistance plus the ~300mΩ of system resistance has to be kept low enough to permit V_{CEsat} and R_{DSon} measurements at the desired high currents.

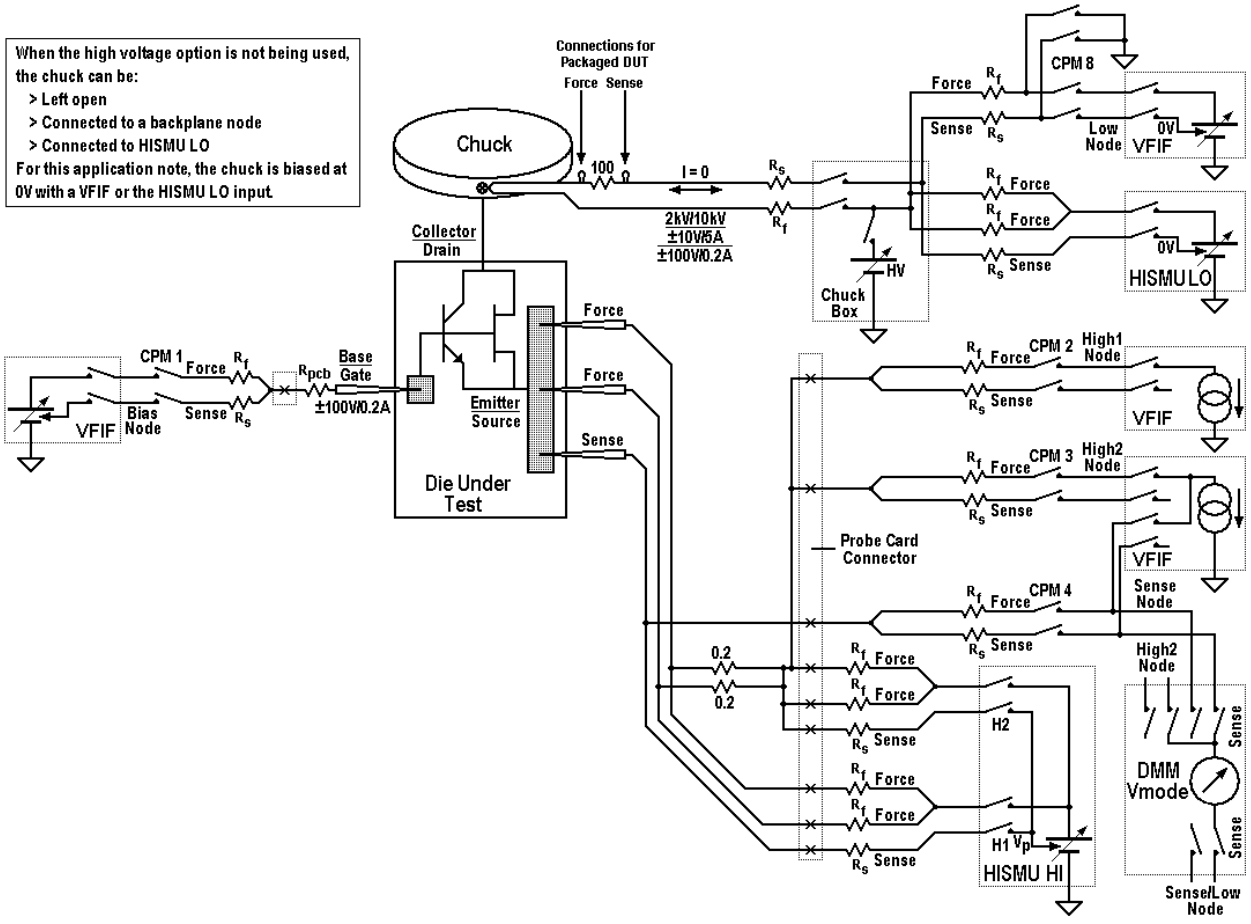


Figure 3 – Probe Card & System Connections for High Voltage Breakdown and Low Saturation Voltage Tests

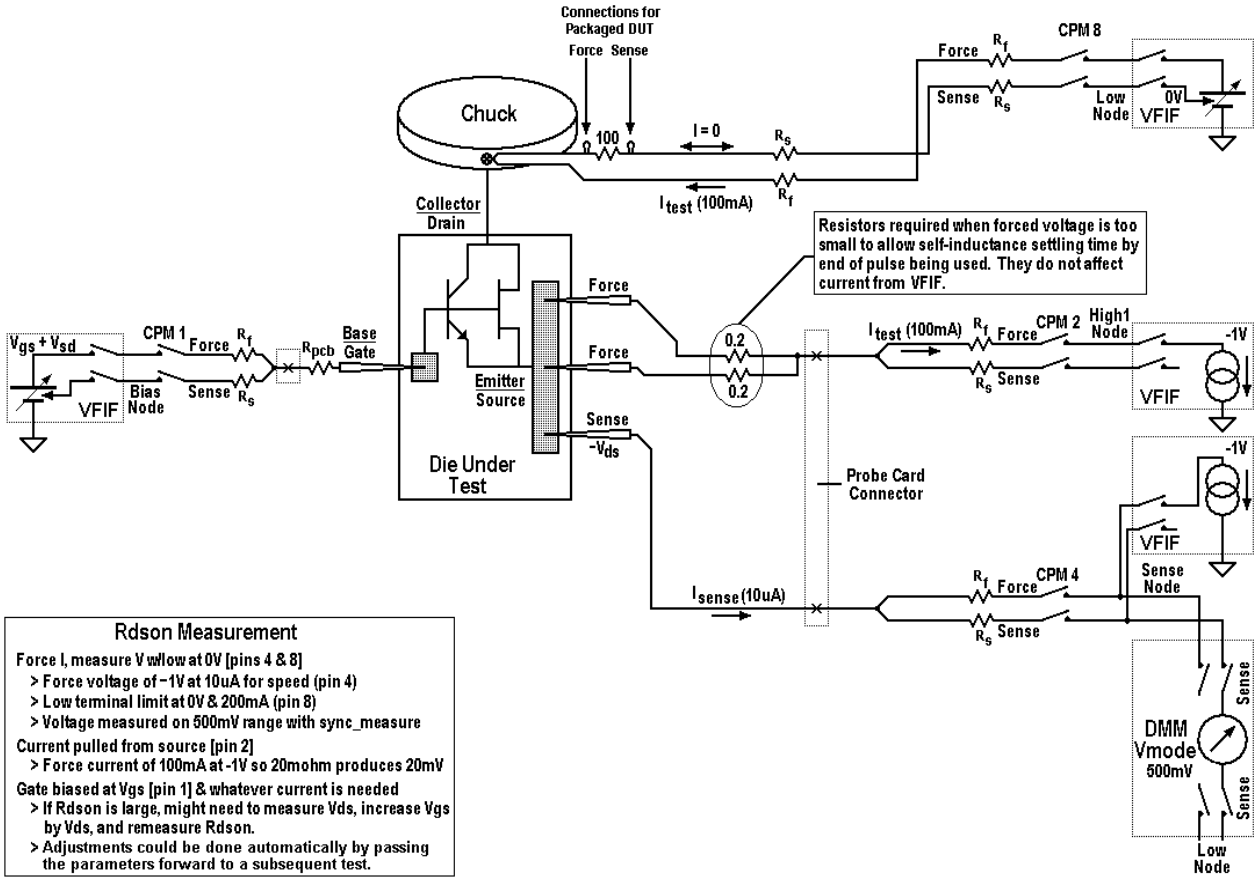
Force I, Low R_{DSon} Measurements

For field effect devices that do not have a separate current dependent voltage term when operating in saturation, a Reedholm system can measure very low channel resistance without having to invoke high currents. Thus, if the channel voltage can be measured accurately enough, low currents are suitable for determining R_{DSon}. And if channel resistance appears different at higher currents, the cause would have to be something like self-heating, changes in bias conditions, etc., and would not imply incorrect R_{DSon}.

Figure 4 was derived from figure 3 by removing connections and resources not involved in making low voltage measurements. The four-terminal test algorithm does not work because there is only one low pin. Fortunately, it is not necessary to write a special test.

Instead, a force I, measure V algorithm, with the low terminal biased at 0V can be used to make the differential voltage measurement. Test current of 10µA is not significant with I_{DS} of 100mA, yet does not incur much delay when using Ilimit bit driven automatic delays.

- Another VFIF forces a large current (100mA) through the channel since the low terminal current limit is automatically set to 200mA.
- A fourth VFIF can bias the gate and turn on the transistor. At 100mA, channel voltage would be insignificant, so V_{GS} would not need to be adjusted to compensate for V_{DS}.
- If thermal emf or other sources of systemic voltage offsets are suspected, the 10µA sense current can be reversed and two readings averaged to eliminate the offsets.
- Line synchronous averaging can be used to take measurements in 25msec.



Rdson Measurement

Force I, measure V w/low at 0V [pins 4 & 8]
- > Force voltage of −1V at 10uA for speed (pin 4)
- > Low terminal limit at 0V & 200mA (pin 8)
- > Voltage measured on 500mV range with sync_measure

Current pulled from source [pin 2]
- > Force current of 100mA at -1V so 20mohm produces 20mV

Gate biased at Vgs [pin 1] & whatever current is needed
- > If Rdson is large, might need to measure Vds, increase Vgs by Vds, and remeasure Rdson.
- > Adjustments could be done automatically by passing the parameters forward to a subsequent test.

Figure 4 – Connections for Low Current Saturation Voltage Tests

Pulsed Current at a Voltage Measurements

Forcing voltage pulse and measuring current works very well when dynamic resistance is fairly large, but achieving a high current requires overcoming modest amounts of cabling self-inductance.

This was not obvious when initial attempts were made to measure the 21.35mΩ wire segment described on page 1. Forcing 100mV should have resulted in ~5A, and polarity reversal should have eliminated possible thermal emf and offset related errors. However, measurements were around 40mΩ. Resistance was higher than expected because current was lower. One reason was that force/sense transistor clamps in the 10kV chuck box changed the sense point, so they were removed and a second 300V spark gap was installed so that matrix and HISMU connections would not be subjected to excessive voltage. But the measurement only dropped to 30mΩ.

It was first thought that the remaining error was due to self-inductance of the HISMU cabling preventing full current before the end of the voltage pulse. Using the calculator at www.consultrsr.com, the 66" length of 26awg wiring produces 3µH of self-inductance. While that level of self-inductance does require more instantaneous voltage while the amplifiers reach high current levels, even the fastest rise time does not induce much voltage. Calculating inductive voltage (V = LdI/dT), shows that it only requires 0.5V to produce 5A in 30µsec.

As shown in figure 5, currents did not reach satisfactory levels due to significant loop gain reductions for the HISMU LO amplifier when the transistor dynamic on resistance is very low. Increasing resistance to 100mΩ allows accurate saturation resistance measurements within 200µΩ by using 200µsec pulses.

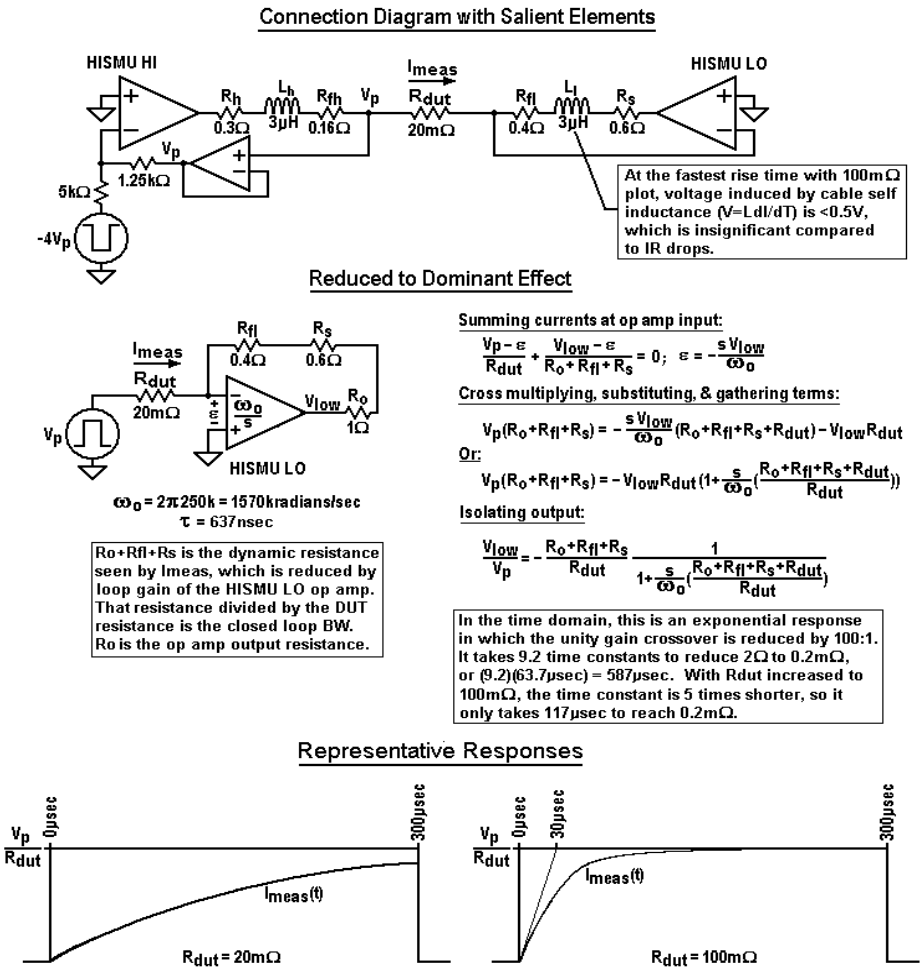


Figure 5 – Connections to Measure Series Resistance

Measuring R_{series} with Voltage Pulsing

If saturation voltage needs to be measured at currents >200mA for transistors having low dynamic on resistance, resistance needs to be placed between the force probes and the sense point for the HISMU output.

As with figure 4, figure 6 was derived from figure 3 by removing connections and resources not involved in making low voltage measurements.

The 4-T test connects the DMM to make a differential voltage measurement across the 200mΩ resistors with CPM pin 3 sensing voltage on one side of the resistors and pin 4 sensing the source voltage through the sense probe. Thus, the measurement includes the probe to pad contact resistance of the two force probes in parallel. In other words, making the measurement

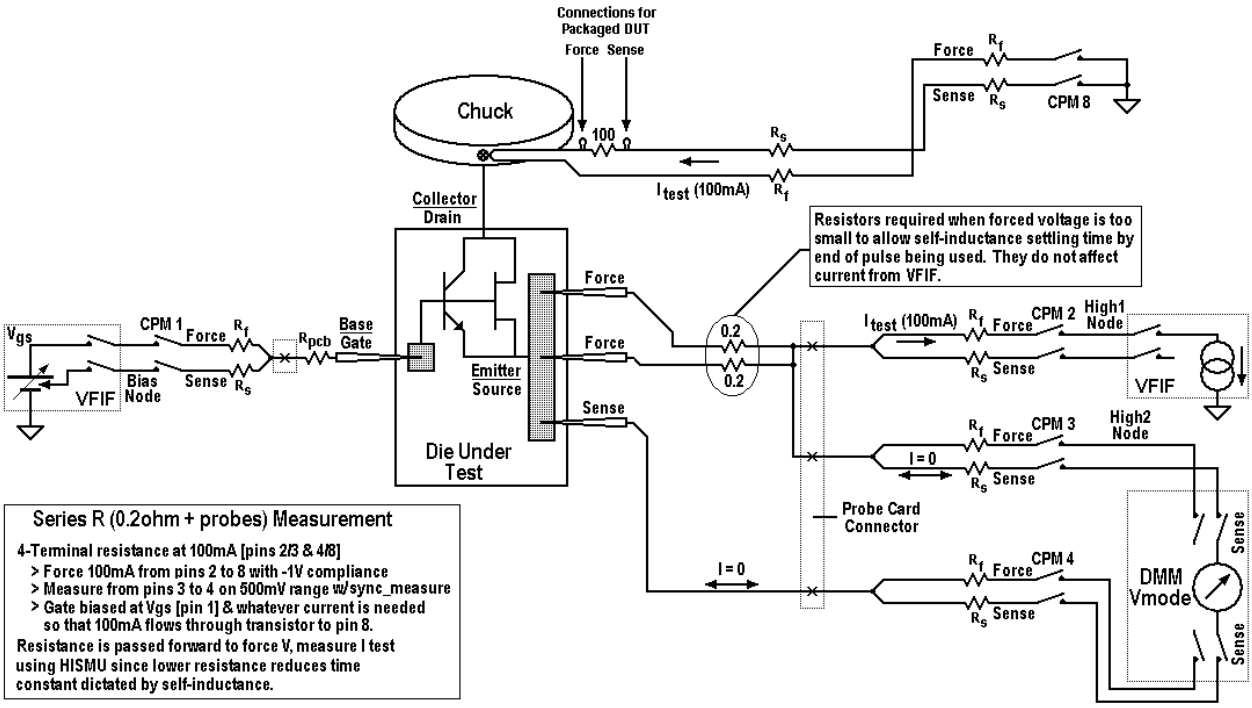


Figure 6 – Connections to Measure Series Resistance

A four-terminal test (4-T) algorithm is used for this measurement with a VFIF biasing the gate/base sufficiently to allow 100mA to flow from pin 8 tied to the drain/collector. Test current is pulled from the high lead through CPM pin 2.

automatically allows systemic errors in addition to compensating for possible shifts in value of the dropping resistors.

By using line synchronous measurements, resistance is measured to the full resolution of the DMM on the 500mV range. Worst-case resistance variability would be limited only by shot noise of the DMM, or <|100μΩ|, and typical variability would be an order of magnitude lower determined by A/D resolution of |7.8μV|.

Putting It All Together

A probe card was modified to accept high voltage transistors with wiring that matches that in figure 3, except that a socket took the place of the probe needle and chuck contacts. Three wires representing the two source and sense contacts were crimped and soldered into the same socket, but that only provides sensing to where the transistor lead plugs into the socket. The 18kV chuck contact cable could not fit into the socket for the drain connection, so it was screwed to a post around 1" from the socket. Voltage drop between drain and post was 500µV with 100mA test current, so that segment contributed 5mΩ to the measurements shown in figure 7. The resultant 7mΩ is reasonable series resistance of 0.5" of #24 wire and two contacts.

An RDS Intranet test plan was written for the test types described in this note, with fairly self-explanatory names shown in the table. Intermediate calculations for bias conditions are not shown. For example, with the drain at 0V, V_{GS} needs to be adjusted for drop across the channel. An enhancement mode, 30A power MOSFET was used for testing. This transistor has very low channel resistance and little mobility degradation at 5A.

Test Result Descriptions

1) R_{series} is the measurement of the paralleled 200mΩ resistors in series with the source.
2) R_{DSon} Low I is the measurement of the channel resistance with the transistor fully turned on. Because Vds is so small even at 100mA, this is resistance with no mobility degradation.
3) V_{DS} Pulse 1 is the computed voltage pulse it should take to produce 5A through the combination of R_{series} and R_{DSon}.
4) I_{DS} Pulse 1 is the current measured during a 200µsec voltage pulse of height V_{DS} Pulse 1.
5) V_{DS} Pulse 2 is the computed voltage pulse corrected for the reduced mobility implied by the I_{DS} Pulse 1 measurement.
6) I_{DS} Pulse 2 is the current produced by 200µsec pulse equal to V_{DS} Pulse 2. This final measurement assures that R_{DSon} is measured at the 5A target current.
7) R_{DSon} at 5A is shown for 100µsec, 200µsec, and 300µsec pulse widths.

Test Name	Last Result	Status	Elapsed Time	Test Time	Average	Minimum	Maximum	StdDev
Rseries	124.069m	0	380m	38m	124.366m	123.912m	125.006m	289.534u
RDSon Low I	33.2124m	0	1.74m	174u	33.2291m	33.2118m	33.241m	10.0365u
VDS Pulse 1	-786.406m	0	1.33m	133u	-787.973m	-791.163m	-785.761m	1.44829m
IDS Pulse 1	-4.91546	0	1.07	107m	-4.92343	-4.94537	-4.90798	9.45879m
VDS Pulse 2	-799.932m	0	1.54m	154u	-800.228m	-800.493m	-799.613m	299.938u
IDS Pulse 2	-5.00021	0	1.07	107m	-4.99896	-5.00021	-4.99024	3.16386m
RDSon 100us	37.685m	0	1.03	103m	37.4807m	36.7417m	37.9548m	322.718u
RDSon 200us	35.911m	0	1.57m	157u	35.7133m	35.0476m	36.1796m	301.968u
RDSon 300us	35.911m	0	1.12	112m	35.6894m	34.9678m	36.1796m	315.585u

Figure 7 – R_{DSon} Measurement Data for Enhancement Mode MOSFET

Analysis Confirmation

Testing validated the previous sections of this note, proving that voltage pulsed measurements of very low RDSon channel resistance is easily achieved with automatic compensation:

1) For ten readings, variability of R_{DSon} Low I had a span <29µΩ and standard deviation of 10µΩ.
2) Mobility degradation of ~2% at 5A was compensated to permit accurate R_{DSon} measurement at 200µsec and 300µsec pulse widths.
3) R_{DSon} was predictably higher at 100µsec due to cable inductance when pulsing 787mV.