DATA SHEET

DS-11103

100kHz Capacitance Meter [100kHz CMM]

- **100pF, 1nF, & 10nF Ranges**
  Resolution of 3.5fF on lowest range
- **16-bit Integrating A/D Conversion**
- **Full-scale Step Response < 2msec**
- **Digitally Synthesized Excitation**
  100kHz ± 0.01% crystal controlled
  15mV or 100mVrms ± 1.0%
  Filtered with tuned L-C tank circuits
- **C-V Bias to ± 250V with HVSMU**
- **Memory Mapped Control**
- **Set and Forget Adjustments**
- **Continual In-line Calibration**
  Compensation includes probe card
  Based on internal reference capacitors
- **Single, 0.75" instrument slot**

Basic Operation

The 100kHz CMM starts measuring capacitance by connecting the DUT between a 100kHz excitation signal and the summing point of an operational amplifier. Current through the DUT capacitance flows through the feedback capacitor of the first amplifier stage, thereby producing ac output voltage proportional to the feedback capacitor. Range capacitors of 100pF, 1nF, and 10nF provide full-scale ranges of 112pF, 1.12nF, and 11.2nF respectively. Excitation can be 15mV or 100mVrms. The input amplifier shown below is followed by three AC gain stages, which feed a synchronous demodulator that presents a filtered dc signal to a 2.5V A/D converter.

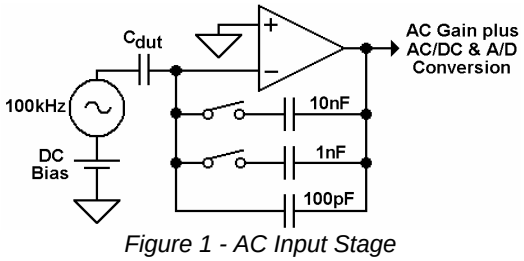

Figure 1 - AC Input Stage

100kHz CMM (P/N 11103)

Range (pF)	Source Error		Resolution (fF)
	Offset[1,2]	% of Value	
100	0.01% of Range	0.02	3.5
1000			35
10000		0.03	350

Comments:

1) Repeatability is within ± 0.01% for stable external conditions.
2) Offset errors based on use of offset compensation.
3) % of value errors are relative to calibration capacitors and include effects of prober analog cable.
4) Measurement accuracy is proportional to range offset error and percentage of value measured. For example, measuring 50pF on the 100pF range results in ±20fF uncertainty span
   C_x = 50pF ± (0.01% of 100pF + 0.02% of 50pF)
   C_x = 50pF ± (10fF + 10fF)
   C_x = 50pF ± 20fF
5) DC voltage biasing to ± 600V has no effect on accuracy.
6) Test frequency is 100kHz ± 0.01%.
7) Test levels are selectable at 15mV or 100mV rms ± 1.0%.
8) Step response to within 0.1% of capacitance change is <2msec.
9) A/D conversions are 50msec.

AC-to-DC Conversion

After amplification, the AC signal proportional to the capacitor under test is converted to DC by a rectifier circuit gated by the excitation voltage. Thus, amplitude and phase of the device current are preserved in the rectified output. That means that the component of current due to DC leakage or series resistance is ignored. After passing through a low-pass filter, the DC signal is applied to an A/D converter for digitization.

A/D Conversion

The A/D converter is a 16-bit Sigma-Delta type having a maximum count of 32767 bits corresponding to 114.8845pF (3.5fF per least significant bit) on the 100pF range. That much over range (roughly 12%) is much greater than other Reedholm instruments, but is needed to accommodate offset capacitance and lgain deviations. A full-scale maximum reading (32767 counts) corresponds to 2.5V at the A/D input.

Set and Forget Adjustments

Potentiometers and variable inductors are adjusted during manufacturing to compensate for multiple error contributors and place operation of the module in a desired starting condition. These set and forget adjustments are not touched again unless a critical component is changed.

No Effect from DC Bias

DC bias is only applied across the capacitor under test. Even if the capacitor were leaky, a guard amplifier at the CMM input absorbs the voltage as well as driving the shield. This eliminates the need to consider effects of conductor-to-shield capacitance on loop gain in the first stage. A series inductor assures that all device current flows into the input amplifier feedback capacitor. Clamp diodes prevent damage from DC bias voltages up to ±600V.

Accuracy Independent of Excitation

Excitation voltage is set within ±1% of nominal at the factory, but its actual value is not critical. It is not measured during calibration and is not a factor in accuracy of capacitance measurements. All that is required is that the excitation D/A output signal be stable between in-line calibrations when the internal standard capacitors are measured. Changes in excitation have a linear relationship with the capacitance being measured, and in-line gain factor calibration precisely compensates for any change in excitation voltage linearly related to the capacitance being measured.

Field Calibration

Calibration is done by measuring response on each range and each excitation level to a pair of external reference capacitors, nominally 100pF and 1nF. Customers are provided with a set of external reference capacitors measured using Reedholm manufacturing standards. Scale or gain factors are stored in the CMMstd.ini file also used for Boonton based CMM calibration. Offsets are not stored because they are a function of factors that do not affect scale factors but that can change with time and temperature.

In-line Calibration

The final calibration step measures three very stable mica or NPO ceramic capacitors (100pF, 1nF, and 10nF) using scale factors based on the external reference capacitors. Those values are the basis for CMM self-calibration performed at least every 15 minutes. As a result, a calibration done after system warm-up has drift characteristics of the internal calibration capacitors, not the collection of components that affect gain. A root-mean-square error calculation following calibration with external capacitors is <±164ppm based on shifts of ±120ppm for temperature over a ±2C° span, ±100ppm for time of one year, and ±50ppm for voltage change between 15mV and 100mVrms.

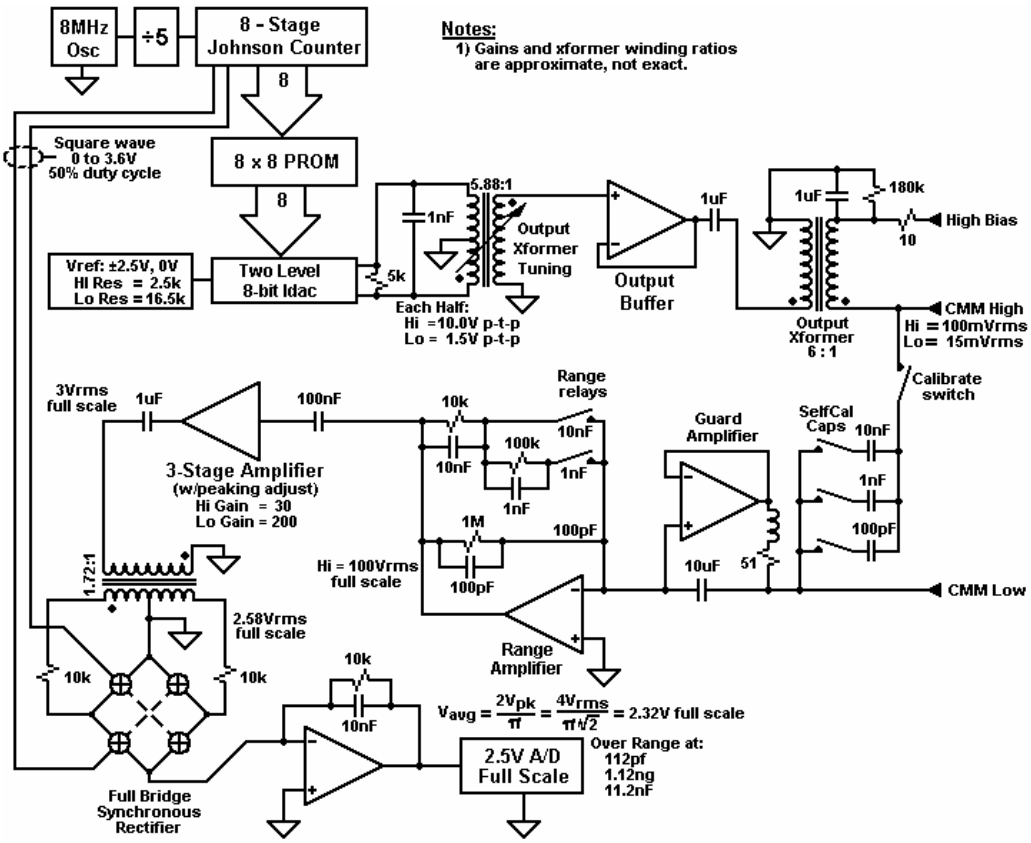

Figure 2 - Simplified Schematic of 100kHz CMM

Measurement Throughput

A single-pole low pass filter formed by the amplifier at the output of the synchronous rectifier determines the time response of the CMM to changes of input capacitance. The oscilloscope output in figure 3 was triggered by having one of the system supplies put out a 1V, 1msec pulse followed by the driver level command to switch to CMM diagnostic mode. This particular image was from connecting a 10nF capacitor with 100mV excitation, but all combinations of diagnostic capacitors and excitation levels generate the same delay and response curve.

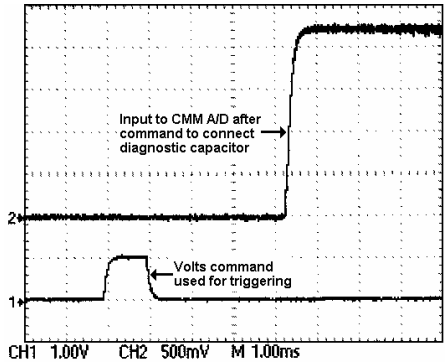

Figure 3 - Response to Capacitance Step

A/D Conversion Time

The 16-bit sigma-delta A/D converter takes 50ms to perform a conversion when clocked at 32.768kHz. A digital low-pass filtering with a 17Hz corner frequency internal to the A/D provides deep rejection cusps at both 50 and 60Hz.

100kHz Signal Generation

A 100kHz sine wave with very low harmonic distortion is produced from a combination of digital synthesis and analog band-pass filtering. A 16-state Johnson counter divides a period of time into 16 equal segments. An 8-bit DAC is programmed as a function of time to produce a 16-step sine wave approximation (figure 4).

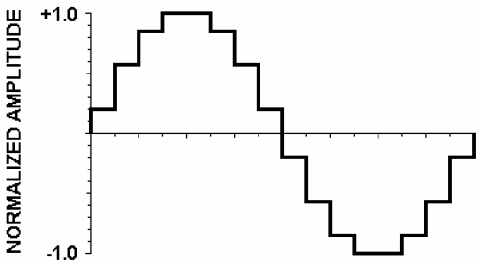

Figure 4 - Synthesized Sine Wave

Harmonic Content and Reduction

If the segment value is made equal to the average value of a sine over the segment time, it can be shown that the first non-zero harmonic is the 15^{th}, the first non-zero harmonic for a 100kHz fundamental is at 1.5MHz. Output of the DAC is applied to a center-tapped transformer that produces a bipolar waveform via induction, and a parallel LC tank circuit based on transformer inductance provides filtering of those harmonics. The net result is AC excitation that depends only on DC reference levels and a crystal clock with none of the stability and sub-harmonic problems associated with analog oscillator derived excitation (figure 5).

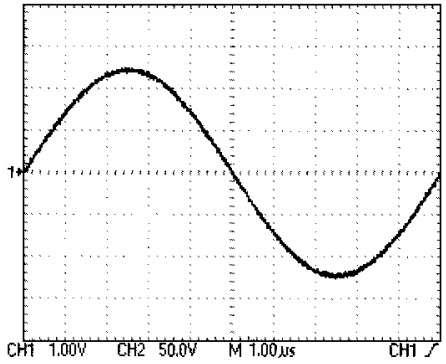

Figure 5 - DAC Output at Tuned Transformer

Phase Adjustment

Compensation for phase shift through the AC amplifiers is done under software control by calling one of 128 data patterns stored in PROM. Each pattern produces a sine wave with a specific phase relationship to the excitation signal. A matching quantify of patterns produces quadrature versions. Each spans a range of 11.3^{o} with an average phase change of 0.089^{o}.

During calibration, a binary search is used for each range and excitation combination to find the byte that minimizes phase shift. Quadrature patterns are used because doing so provides an order of magnitude more sensitivity in selecting the right phase pattern.

Compensation for Limited DAC Resolution

Magnitude of the fundamental 100kHz component varies slightly (± 0.75%) due to the limited adjustment resolution of the 8-bit DAC used to create the sine wave, but the level is very stable. As a result, in-line calibration assures accurate measurements despite slight changes in DAC levels.

Module Control Bit Map

Addr	Function	MSB	Data Byte						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
00	Status	HV	1	1	0	X	X	X	X
01	Range	100mV	X	X	C(/G)	10nF	1nF	100p	X
02	MSB	B1	B2	B3	B4	B5	B6	B7	B8
03	LSB	B9	B10	B11	B12	B13	B14	B15	B16
04	N/A	X	X	X	X	X	X	X	X
05	Phase	A16	A15	A14	A13	A12	A11	A10	A9
06	Output	D10n	D1n	D100p	CMM-	X	CMM+	CMB+	Diag
07	N/A	X	X	X	X	X	X	X	X

Notes

1) Status Byte
   - This is a read-only byte. Writing to it initiates A/D conversion.
   - Bits D6 and D5 are hard-wired to "1" and bit D4 to "0" for differentiation from Boonton based CMM's.
   - Bit 7 is hard-wired to "0", but is easily changed to a "1" if the module is modified for 2kV operation.
2) Range Byte
   - Excitation is 15mVrms unless bit D7 is high, which signifies 100mVrms excitation.
   - Bit D4 is actually the highest bit of the phase control word, so there are actually 256 unique phases. If bit D4 is high, measurements are made in phase with capacitance signal. If low, phase is shifted 90° and used during calibration to assure that the proper phase is used during capacitance measurements.
3) Data Output
   - Both bytes are read only. Writing to the MSB byte initiates an A/D calibration cycle.
   - ADC data output is offset binary coded

	At ADC	
+Full Scale	= 11 - 1	= FFFFH
Zero	= 10 - 0	= 8000H
-Full Scale	= 00 - 0	= 0000H

4) Phase Byte contains the address of the PROM program used for phase adjustment. If bit D4 of the range byte is high, the five address bits (D3 to D7) select a capacitance measurement waveform. If bit D4 is low, the address selects a waveform for conductance measurement that shifts the phase by +90°.
5) Output Byte
   - High signals on bits D5 to D7 connect internal diagnostic capacitors (10nF, 1nF, 100pF) if bit D0 is high.
   - A high on bit D4 connects meter low to node 4 for sensing device under test currents.
   - A high on bit D2 connects meter high to node 2 for delivering excitation voltage to the device under test.
   - A high on bit D1 connects the bias input to node 1 so that a power supply can send voltage to the meter high terminal and bias the device under test.