

# Overview: 0.35 $\mu$ m Test Chip Project

---

**REEDHOLM**  
Georgetown, TX 78626      Tel: 1.512.876.2268  
[sales@reedholm.com](mailto:sales@reedholm.com)      [www.reedholm.com](http://www.reedholm.com)

---



































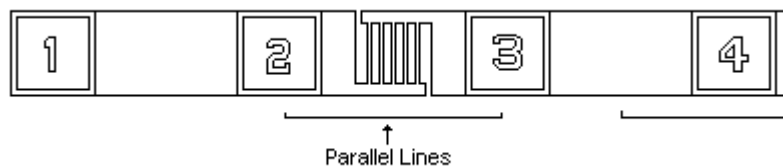






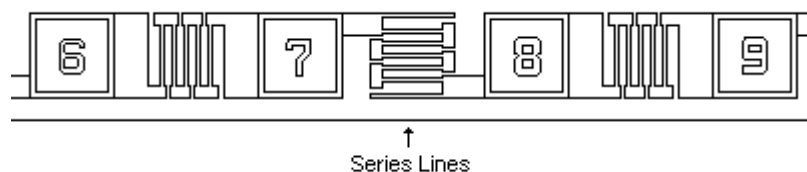
## Stress Migration

Stress migration remains of significant importance to semiconductor processing, and structures are designed for highly accelerated testing for this mechanism. However, there is questionable payback for the space and time allocated for such structures. This is primarily due to the related failure mechanism physics. Stress migration is heavily time dependent. Propagating tensile stresses due to thermal mismatch between oxides and conductors into voids can take weeks. However, if voids do occur and are present at the end-of-line testing where these WLR structures would be monitored, the test structure will highlight them.



*Figure 11 - Stress Migration Reference Structure*

To detect the presence of voids, the test compares time-to-failure values from a reference and monitor structures for a given metal layer. The reference structure contains multiple identical segments in parallel to minimize the impact from a void that could be present within the reference area (Figure 12). This simple arrangement shunts current around a potential void laden reference segment. The monitor consists of identical size test segments arranged in series with alternating X and Y orientations (Figure 12). This prevents the structure from having wafer placement sensitivity due to any radial stresses.



*Figure 12 - Stress Migration Monitor Structure*

Techniques utilizing a ramped breakdown method cause catastrophic failure and prevent effective analysis of the failure location. To address this undesirable result, a time-to-failure method can be more effective in detecting line voids. This approach also allows stress to be halted before full opening of the test line in order to preserve the void and allow failure analysis.

## Chapter 6

### Summary

The advantages of a well developed, mature WLR program have been touted through the years, but these benefits have not been easily replicated. The efforts of individual foundries to use these designed experiments to demonstrate structure effectiveness and statistical data will assist in verifying WLR's value as a process monitor. Thus, the FSA project proliferates the use of Reedholm WLR structures and test methods for semiconductor process that is significantly advancing WLR as a technology.

## Chapter 7

### References

---

- <sup>1</sup> F. Kuper, et al, "Relation Between Yield and Reliability of Integrated Circuits: Experimental Results and Application to Continuous Early Failure Rate Reduction Programs," *1996 International Reliability Physics Symposium*
- <sup>2</sup> A. Papp, et al, "Use of Test structures for a Wafer-Level-Reliability Monitoring," *1996 International Conference on Microelectronic Test Structures*
- <sup>3</sup> S. Garrard, "Production Implementation of a Practical WLR Program," *1994 International Integrated Reliability Workshop Final Report*
- <sup>4</sup> A. Papp, et al, "Implementation of a WLR-Program into a Production Line," *1995 International Integrated Reliability Workshop Final Report*
- <sup>5</sup> Fabless Semiconductor Association WLR Committee Charter, 1995
- <sup>6</sup> J. Shideler, "A Model of a Wafer Level Reliability Program for a Large Corporation," *1991 International Integrated Reliability Workshop Final Report*
- <sup>7</sup> G. Madson, et al, "Building Reliability into an EPROM Cell Using In-line WLR Monitors," *1995 International Integrated Reliability Workshop Final Report*
- <sup>8</sup> J. McPherson, "Does Building-In Reliability Imply More or Less Wafer-Level Reliability Testing?" *1996 International Integrated Reliability Workshop Keynote Address*
- <sup>9</sup> Case Histories of WLR Payback, SGS Thomson and National Semiconductor
- <sup>10</sup> EIA/JESD35-1 EIA/JEDEC Standard, "General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics."
- <sup>11</sup> EIA/JESD35 EIA/JEDEC Standard, "Procedure for the Wafer-Level Testing of Thin Dielectrics."
- <sup>12</sup> S.U. Kim, "A Test Structure for Plasma Process Charging Monitor in Advanced CMOS Technologies", *1996 International Integrated Reliability Workshop Final Report*
- <sup>13</sup> Satish Menon, et al, "A Candid Comparison of the SWEAT Technique and the Conventional Test Procedure for Electromigration Study in Sub-Half Micron ULSI Interconnects." *1997 International Integrated Reliability Workshop Final Report*
- <sup>14</sup> M. Dreyer, P. Ho, *Handbook of Multilevel Metallization for Integrated Circuits*, S. Wilson, C. Tracy, ed., 1993 p. 595.
- <sup>15</sup> Greg Petter, "Accuracy Enhancement in Electromigration Measurements," *1998 VLSI Multilevel Interconnect Conference*
- <sup>16</sup> I. A. Blech, "Electromigration in Thin Aluminum Films on Titanium nitride," *Journal of Applied Physics*, Vol 4, April 1976