

**One Right Answer
for
Production E-Test**

REEDHOLM

Georgetown, TX 78626
sales@reedholm.com

Tel:1.512.876.2268
www.reedholm.com

Table of Contents	Page
Chapter 1: DC Production Parametric Testing Overview.....	5
DC Production Parametric Test System Suppliers	5
Objectives in Technology Development E-Test	6
Objectives in Production E-Test	6
Problems with Technology Development Transfers.....	7
Problems with Latest Technology Development Systems.....	8
Chapter 2: Production E-Test Changes Slowly	11
Obsolete and New Testers Take Same Data	11
Testers are Independent of Wafer or Feature Size.....	11
Complex Structures are Measured with Simple Tests	12
Instrument Specifications Are Overkill	12
Chapter 3: New Paradigm for Production Parametric Testing	13
Few, if any, Design Parameters	13
One True Result for Each Parameter	13
Critical or Scrap Parameters	14
Monitor Parameters.....	14
What Isn't Production E-Test?	14
Agilent 4082A Development System Ill-Suited for Production E-Test	16
Chapter 4: Using Reedholm Testers in Production E-Test.....	19
Variety of Cabinets - Same Instrumentation.....	19
Eliminate Risk of Obsolete Test Platforms.....	20
Bring Production E-Test Under Control	20

Table of Contents (cont.)	Page
Use Less Floor Space	21
Increase Productivity.....	21
Stories from a Few Satisfied Customers	22
Chapter 5: Reedholm Production E-Test System Features.....	23
Typical 24-Pin Configuration	23
Enhancements	24
Data Driven Software.....	24
No Obsolescence – Timeless Systems	24
Device Test Oriented Software	24
Software Configuration Control.....	26
Memory Mapped I/O Control	27
On Demand Optimization Tools	28
Software Bottleneck is Eliminated.....	29
Chapter 6: Getting Started with Reedholm.....	31
No Risk Evaluation Using Tested Wafers	31
Implementation After Order Placement.....	31
Installation.....	32
Continual Improvement	32

List of Illustrations	Page
Figure 1 - Latest Agilent Development System.....	16
Figure 2 - 4280A Specification Sheet with Comments	17
Figure 3 - Multiple RI-40's for 200mm Wafers	19
Figure 4 - RI-EG for 150mm & Smaller Wafers	19
Figure 5 - RI-70 Cabinet for Up to 600 Pins	19
Figure 6 - 100% Coverage of Each and Every Wafer	21
Figure 7 - RI-EG Intranet Configuration	23
Figure 8 - Gradient (Slope) Overlaid on Vgs Transfer Curve	25
Figure 9 - Reedholm Test Control Hierarchy	26
Figure 10 - Instrumentation Memory Map	27
Figure 11 - Timing Output for PNP Latchup.....	28
Figure 12 - Source Code is Different than Reedholm Data Driven Approach	30

Chapter 1

DC Production Parametric Testing Overview

Upwards of 1000 facilities worldwide do semiconductor wafer processing. Of those, around 500 produce wafers with functional devices that wind up being used in electronics gear. Around 2000 parametric testers are used in those sites, 750 of which are obsolete. That is, the system vendor has stated they no longer provide new versions, no longer update software, and will only repair on a best-effort basis. Obviously, the failure of any obsolete system in a production setting can have catastrophic effects on wafer output.

Except for simple devices such as diodes and transistors, wafer fabrication depends on taking dc and capacitance data from simple test structures consisting of diodes, resistors, capacitors, and transistors strategically placed across the wafer. Production parametric testing provides proof that manufacturing processes are under control through the measurement of those simple test structures, collectively known as process control monitors (PCM's). Properly designed, PCM's produce information on the quality of major process steps and their interactions.

Integrated production parametric test systems are a collection of computer-controlled instruments and software for creating tests, controlling probers, formatting data, and interfacing with corporate networks. They are used to gather data from PCM's, with much of the results being individual data points for each parameter (V_t , H_{fe} , BV_{dss} , R_{on} , etc.). As a new process is developed, entire wafers are covered with a combination of PCM's and functional test vehicles. Testing is done by technology development using test plans that often have thousands of results.

As the process is brought under control, fewer PCM's are placed on the wafers. By the time of transfer to production, a few PCM's are tested per wafer with each PCM representing a proportional amount of the wafer. Thus, there might be 5 sites on a 150mm wafer, 9 on a 200mm one, and 17 on 300mm wafers. In production, some companies rely on PCM's that are placed in locations that could have product die, and others put PCM's into scribe lanes between product die. That level of coverage is called 100% testing when done for every wafer in a lot.

DC Production Parametric Test System Suppliers

In February 2009, prompted by an unprecedented downturn in the semiconductor industry, Keithley announced that it would no longer supply integrated parametric test systems. Customers who knew of the impending loss of support for S900 and S400 models in 2010 were told that the latest S600 models would not have support starting in 2012.

In the consumer electronic world, five years means two or three generations of products. In production e-test, five years is barely enough to get started. Some parametric testers have been in continual use for over 20 years.

Replacing the obsolete Keithley systems doesn't require new measurement capability. Production management have long been satisfied with capabilities of systems offered by Agilent, Keithley, and Reedholm, so new measurement capabilities are not important when obsolete testers are replaced with supported ones. In an attempt to stay in the game, Keithley claims that test code from the obsolete systems can be easily ported to roll-your-own test systems now made up of Keithley components.

Agilent and Reedholm are now the only suppliers of turnkey, integrated parametric test systems. Like Keithley, Agilent markets to technology development. That approach works as long as new fabs are being built. Although these talking points do not bear up to analysis, they were used so much that they must have been successful in obtaining orders from new fabs:

"The tester needed for 200mm, 300mm etc"

"1fA (or 1fF) sensitivity for the next technology node"

Compared to the cost of a new fab, parametric testers and probers are virtually free, so buyers are not budget constrained when outfitting testers for new fabs. Promising the moon in measurement capability worked because no one wants to risk buying a tool that is inadequate. Not having rigorously controlled test algorithms was not a problem because customers wrote or modified 90% of algorithms provided by Agilent or Keithley.

Objectives in Technology Development E-Test

Parametric testing in technology development obviously has to be responsive to development needs. Test speed is not critical as long as data is available within a day or so of the final process step. What matters is that test plans can be created or modified very quickly. It does not really matter if excessive delays and averaging are used to make sure that critical parameters are measured correctly. Also, some measurements are made that would be way too slow to make in a production environment. For instance, instead of measuring leakage currents to assure channel pinch-off or oxide integrity, actual leakage current might be specified as a critical need in development regardless of how long the measurement took.

Because an overwhelming amount of data is produced during development, and because outlier data can be ignored in development, not all tests have to work properly. Also, test structures with flawed designs have to be tested even if standard test algorithms do not work correctly. For instance, a structure with sneak paths to other pads would be redesigned before reaching production. But, until then, it might have to be used to gather critical process information. Being able to create and use custom tests for abnormal devices makes sense in development.

Such a disparate array of system requirements pushes the parametric testing envelope, so test systems with lots of bells and whistles are purchased for development just in case one of those invented features might be needed.

Objectives in Production E-Test

On the other hand, production parametric tests change slowly and do not push the testing envelope. The application defines what is needed. Measurements made today are largely unchanged from those made 30 years ago. In effect, test structures evolve through the development process to match what has proven to be effective in controlling previously released

processes. Thus, structures that might have required sub-pA or sub-pF measurements during development are scaled so that good data can be gathered in a few milliseconds instead of seconds. Furthermore, it is not unreasonable to require that all tests released to production execute in <100msec.

In production, cost is paramount as long as control is assured. That means the solution with smallest possible footprint and highest throughput is best as long as testing coverage addresses the application.

- Several sites need to be tested on every wafer to identify bulls-eye yield drops and zero-yield wafers. Modern processing tends to blur lot dependence, so statistical area sampling is seldom valid. Without such 100% coverage, process problems are passed to the back-end and incur even higher costs.
- Tests need to generate true results useful in monitoring or improving yield.
- Software needs to have the same configuration control as other manufacturing activities.

Problems with Technology Development Transfers

Most semiconductor manufacturers operate with a compromised production parametric test operation. Typically, technology development groups create test plans with thousands of parameters that produce a combination of process, design, and device modeling data. So much data is taken during development that optimization from a quality or speed perspective is seldom considered until it is time for parametric testing to be transferred to production. By then, it is assumed that the best approach is to start out using the same test plans and testers in production. This is problematic on several levels:

- Product engineers inherit slow, bloated test plans, yet do not have time to optimize tests for production. They are too busy sustaining previously released test plans. Once volume picks up, the bloated, slow test plans become a bottleneck that is often addressed by frustrated management dictating an arbitrary reduction in the quantity of tests.
- Development focused parametric testers have measurement features that do not matter to production e- test. Two recent examples are RF measurements and multi-frequency capacitance meters. Buying development testers for production wastes money on measurement frills seldom, if ever, used in production.
- Because speed is never an issue, development groups spend money for measurement resolution that is unrealizable in volume testing, and unimportant in production. An example is buying testers promoted as having fA, or even aA, sensitivity, when the lowest production pass/fail decisions are made at tens of pA.

When the Agilent and Keithley development test plans are transferred to production, bottlenecks almost always appear because tests are not characterized or optimized for accuracy and speed. Test times are incredibly high compared to what they should be, regardless of test system vendor. In head-to-head evaluations, Reedholm systems have been 2X to 7X faster. Almost all of that is due to lack of diligence at the time of transfer to production. After the transfer, no one has time to work on bottlenecks or accuracy.

Software is Uncontrolled and Almost Uncontrollable

In addition to being slow, test software delivered to production is uncontrolled. Unfortunately, it stays uncontrolled, so in many fabs production e-test might be the only production activity that does not have configuration control or revision history.

As long as there are no test problems or changes in tests, lack of configuration control is not an issue. But changes are a fact of life, and tying test data shifts to test code changes is close to impossible. It essentially falls to what the parametric test engineer can remember.

Accuracy is not the Highest Priority

Accuracy is another problem with transferred test plans. Critical (pass/fail) parameters are usually accurate and repeatable right away because wafer lots are dispositioned on them. However, monitor parameters taken for possible yield troubleshooting are not well characterized. In evaluations done by Reedholm, 15% of monitor parameters are incorrect. For example, leakage measurements are sometimes taken too soon for currents to even start changing, breakdown results are reported even though a forcing supply has reached compliance, and breakdown measurements do not take into account current being diverted to another part of the test structure.

None of those mistakes affect yield, but they waste time and resources during testing and during analysis. Inaccurate tests should be fixed or deleted instead of being ignored.

Lack of Tools to Assure Accuracy

Surprisingly, test characterization is not easy to do on testers targeted for technology development. Each test type should have one or more device characterization sweeps associated with it. For example, current gain measurements should provide collector characteristics and Gummel plots at the click of a button. Breakdown tests, especially ones done with low currents, need current or voltage versus time tests to determine how long delays need to be and how much averaging to use.

Without easy to use characterization tools, it is easy to understand why tests are not properly characterized before transfer to production.

Problems with Latest Technology Development Systems

To recount, production e-test goals are seldom met when technology development software is transferred to production. Without in-depth review and test plan improvements, transfers cause testing bottlenecks unless an inordinate number of test systems are acquired. With the recent economic downturn, there has been pushback on poor throughput. Rather than deal with the fundamental issue of technology development tests being poorly characterized and slow, new Agilent systems propose to put band-aids on the problem by promising:

- Adaptive sampling.
- Multi-threaded, parallel testing.
- Single-pass testing for DC and RF parameters.

Adaptive Sampling is Still Sampling

Adaptive sampling is slightly more palatable than pure sampling, but still risks moving low yielding and/or unreliable functional die to final test, and eventually to customers. That is a high price to pay for deficiencies in control of production e-test. In these days of single wafer processing, parametric testing needs to have good coverage of every wafer being produced.

Multi-tasking/Parallel Test Still does not Belong in Production E-Test

Parallel testing smacks of attempts 20 years ago to convince users to multi-task a single set of instruments among multiple probers. That died out because test times per touchdown were not the speed limitation in production e-test, and that is not the fundamental limitation now.

Furthermore, since there is little duplication of devices in production PCM's, simple parallel testing of similar devices does not apply. For multi-tasking to work, multi-threaded software has to be used so that multiple faster tests can execute simultaneously with slower ones. In addition, test structure layouts have to be compatible with a specific test system model.

If excessive delays and unnecessary averaging did not bloat test times, average test time per device would be too short to even consider the extra costs in complexity, software development time, and test structure layout time.

At first glance, multi-tasking tests might have a role in technology development when similar devices are often placed in the same test structure, and have similar test conditions and test times. However, multi-tasking test software is not easy to do, so it takes much longer to create test plans. Since throughput is not an important criterion in technology development, there is little reason for technology development engineers to use multi-tasking tests.

Realistically, multi-tasking tests can be a boon in slow wafer level reliability testing when sites are probed for minutes or hours. But slow WLR hardly needs the speed and flexibility of a production e-test system. That application is best served with dedicated tool sets, not ones that cost \$600,000.

Additional Bottleneck from Combining DC and RF Testing

Combining DC and RF in production testing might be good for Agilent, but does not help production fabs that make both types of wafer measurements. Before the economic downturn, Reedholm bested Agilent and Keithley in head-to-head competition at a GaAs integrated device manufacturer that had previously decided to use a combined DC/RF system for parametric as well as RF testing.

While the replaced Agilent system met its specifications, getting good RF data with a probe card interface that worked well at DC required RF recalibration each time the card was changed. That caused such a bottleneck that a Reedholm tester was evaluated. It was so much faster that two Reedholm testers were able to replace five obsolete HP testers. Furthermore, data was more reliable.

RF test is done with the Agilent DC/RF system after wafers have been qualified on the Reedholm systems. Calibration is still required for each unique RF system probe card. But at least the bias tees do not impact DC test data. In hindsight, the company could have put together a standalone RF system for far less money, but the Agilent DC/RF system had already been purchased.

Empty Promises of Laboratory Results on the Production Floor

In addition to the features that purport to deal with technology development tests being poorly characterized and slow, Agilent promises to provide laboratory measurements on the production floor.

One implication of the claim is that test structures cannot be scaled for fast, accurate measurements. Another is that the Agilent system produces lab results. The latter is elaborated with marketing hype on the Agilent brochure promising 1fA and 1fF sensitivity. A closer look at the specifications shows guaranteed performance 500 to 1000 times worse.

Regardless, even with the utmost care, it is not possible to reach fA and fF with an integrated tester and probe card because probing parasitics overwhelm real device values. That is, if one were trying to measure the true gate capacitance of a small device, the probe pad and probe card capacitances would overwhelm it.

Whether Agilent testers operate down to 1fF or 1fA is immaterial from a production standpoint. If there is a need to measure 1pF or 1pA because a test structure device is too small, it needs to be scaled to a larger size before release to production. Otherwise, the parameters will be too problematic to be brought under control.

Chapter 2

Production E-Test Changes Slowly

Unlike functional testing of communications, digital, and memory devices, production e-test needs change very slowly. Tests from 30 years are still being run today and still work. Process control monitoring structures provide information on thicknesses, doping levels, device widths, etc. Structures are very simple, and have not changed much in the past 30 years:

- Capacitors are still capacitors.
- Diodes are still diodes.
- Resistors are still resistors.
- Transistors are still transistors.

Obsolete and New Testers Take Same Data

Fab managers with several generations of test systems know that production e-test changes slowly. It is not unusual to see three generations of test systems in use, with obsolete 20-year-old testers making the same measurements and operating with the same limits as the latest and greatest models.

It isn't that the latest models cannot make better measurements – they obviously can. But all of the energy and effort in designing and marketing them is largely wasted because production e-test needs have hardly changed over the past 30 years.

Testers are Independent of Wafer or Feature Size

Although Agilent and Keithley tout testers matched to wafer sizes or technology nodes, the claims are empty.

Structures Have to be Scaled for Accurate Parameter Extraction

When done correctly, test structures are scaled to be good monitors, and are not representative of in-circuit devices. Even with minimum size transistors, adding probe pads distorts true behavior. Parametric testing cannot get at true transistor behavior at the latest nodes, so there is no justification basis of needing special measurement capability for smaller features.

Ironically, with the latest technologies, thinner oxides have meant that more current, not less, flows in properly constructed devices, so the touted need for "1fA" resolution had no validity.

Wafer Size Only Matters for the Prober

There is no relation between test system capabilities and wafer size. A different prober is all that is needed when going from 75 to 300mm. Tester requirements depend only on the parameters being measured, and those change little over time.

Complex Structures are Measured with Simple Tests

Thirty years ago there was no need for measurements of more complex structures like contact chains because only one metal layer was used. But sheet resistances were measured as well as line widths. And a contact chain measurement is just a resistance measurement with consideration for high resistance and local heating. This is one of many examples in which additional structure complexity does not require new test methods.

Instrument Specifications Are Overkill

Semiconductor process parameters are not well controlled compared to test and measurement instrumentation capabilities. Even parameters that are within a $\pm 5\%$ span have several decades greater uncertainty than production e-test systems. For example, parametric test system uncertainties in 1980 were $\pm 0.05\%$, or 100 times better. Now uncertainties are down to $\pm 0.01\%$ today, or 500 times better. Those are striking ratios when the rule of thumb for control of random variations is that measurements be 5:1 better than the process parameters.

Similarly, process parameters are more sensitive to temperature than instruments. Typically, process parameters vary by $>0.3\%/C^\circ$, so temperature control of $\pm 1C^\circ$ creates errors 30 times greater than modern test system specs.

Chapter 3

New Paradigm for Production Parametric Testing

Wafer acceptance testing can be done with more rigor, at lower costs, and at higher speed if production goals are defined independently of technology development. Breaking the umbilical cord from technology development can improve throughput without sacrificing 100% coverage. By properly characterizing each test released to production, critical parameters, i.e., those with pass/fail limits, will be tested faster. Furthermore, only monitor parameters that are useful in yield troubleshooting or yield improvement should be carried into production.

Few, if any, Design Parameters

While functional device performance is the ultimate reason for processing wafers, yield of functional devices does not provide direct process control feedback. Nevertheless, some foundries do provide functional device performance data as well as process parameters. For example, the MOSIS service (www.mosis.com) includes a ring oscillator structure that has enough elements and a frequency divider that the oscillator output can be routed through any production e-test system. The ring oscillator measurements provide valuable information for foundry comparisons, and the output frequency can be used for wafer acceptance, but unlike a true process parameter, a failure does not point toward a particular process step, or steps. Because functional testing does not provide actionable process information, adding them should be a well-justified exception.

One True Result for Each Parameter

There is only one right value for every test structure measurement, and it cannot depend on tester model, serial number, or type of instruments. If there is no self-heating, buried gate control, and no interference from light, wafer level measurements can only depend on test conditions. When doing correlation, agreement should be extremely good, at least compared to process variability, unless test conditions stress the device and/or cause breakdown. Of course, the high temperature dependence of semiconductor parameters means that wafer temperature has to be under tight control when checking correlation between testers. For example, a 1C° difference between two chucks could easily mean >1% difference in resistivity, threshold, etc.

If the test system does not have built-in, easy to use device characterization software, finding the right answer can be difficult. Taking the wafer to a curve tracer with three or four micro-positioners is hardly adequate. The test system cables are connected to all pads at a test structure site, and it is often the extra connections that make correlation among testers problematic. At best, sneak paths through the site have to charge unused cable capacitance and thus require longer delays. At worst, capacitance loads can lead to latch-up that does not recover until the test is over and power is removed.

Critical or Scrap Parameters

These are sometimes called "go—no go" parameters whose input variables should be under strict configuration control. There are between 10 and 50 scrap parameters. Passing them assures adequate functional yield. Foundry contracts are based on these parameters, and customers can negotiate additional tests for additional costs. Over time, parameters are added as needed to unambiguously detect low yield wafers.

Statistically significant failures cause lots to be held for dispositioning because functional device yield might be too low and/or because device reliability might be affected. While the ultimate goal is for wafers to be scrapped when there are statistically significant failures, scrapping wafers is the province of top management who rely on personal experience, yield/quality projections, and advice from product engineers charged with analyzing results.

Monitor Parameters

These parameters (typically 50 to 300), are taken along with scrap parameters. They guide process troubleshooting during lot dispositioning and are early warning indicators of process shifts that might eventually cause yield drops if the process is not adjusted.

However, lots are not dispositioned using these results, so limits are often not applied or are ignored. Nevertheless, they often provide the only clues when there are yield problems, so they need to be measured accurately. Technology development test plans often have many useless tests when released to production. In evaluations done by Reedholm, 10 to 20% of monitor parameters produce meaningless results.

When low yielding wafer lots escape scrap screens, monitor parameters that correlate with the yield drop are promoted to scrap status by adding appropriate limits and using its status in the wafer lot pass/fail calculations.

What Isn't Production E-Test?

Tests that do not provide actionable feedback on processes or process interactions are sometimes run on production e-test systems. The following paragraphs lists some of them.

Integrated Device Measurements

Measurements of integrated devices such as ring oscillators, memory cells, and ESD protection can flag yield problems, but one or more of the process specific tests should have flagged the problems as well. Because numerous process variables interact, yield of a specific device can be high when a process parameter is clearly out of control. Furthermore, not enough sites can be tested to provide statistics for yield projections.

Process Improvements

When development testers are tied up for new product development, production e-test systems are used for process improvements and yield investigations that are otherwise development activities. If scribe line structures are richly populated, this is done on production wafers. Otherwise, test wafers are run.

Device Modeling

Production e-test systems are well equipped to gather I-V sweep data for device modeling, and it makes sense to monitor channel lengths and widths with a couple of transistor sizes, but taking device modeling data on every wafer and every lot seriously impacts throughput without an increase in modeling data quality.

Process Reliability

Other than a few highly accelerated wafer level reliability tests that execute in well under one second, WLR tests are done at low stress levels that can take minutes to days, and are seldom tied to a specific wafer lot. Testing does not have to be fast, and automatic wafer handling is seldom needed. While a production e-test system can be used for wafer level reliability tests, attributes of speed, automation, and databasing are not tapped. Process reliability tests are best done with a tester and prober combination dedicated to the task.

RF Wafer Measurements

Putting RF capability into a production e-test system dramatically reduces dc measurement accuracy because bias tee isolation resistors make it impractical to use Kelvin sensing. Throughput is hampered because merely changing a probe card requires recalibration of the RF sub-system before dc testing can start on a new product.

Some semiconductor materials can have poor yield at high speed despite passing dc screening, and packaging can also degrade performance. That is why devices have to be individually tested at speed after packaging. However, it does not make sense to package large quantities of devices when there is a process drift that affects all of them. So wafer level RF tests are needed, but those can be done with an RF instrument set and a semiautomatic prober that augment high-speed screening using production e-test systems

Exotic Lab Tests

Despite marketing pushes by Agilent and Keithley, being able to make laboratory measurements on a production e-test system is no reason to actually make them. Such tests are inherently slow, and usually only measure the system itself. For example, the flattening seen in sub-threshold tests is seldom a device characteristic; instead, it is a signature of the system, probe card, or lack of adequate timing delays.

Only those tests that can be used for process control should be transferred to product. Here are some of the tests that are so problematical that they should never be used for wafer lot dispositioning:

- fF Capacitance, which really means <1pF.
- fA Currents, which really means <1pA.
- Multi-frequency capacitance.
- Charge pumping.
- 1/f noise.

Agilent 4082A is Development System Ill-Suited for Production E-Test

The 4082A is expensive at 200% more than a Reedholm tester. Plus it requires an expensive prober plus an expensive handler because of the heavy test head. As a result, the larger footprint takes a lot more expensive clean room space, and more time for operators to change probe cards.

Because Agilent does not provide device oriented test plan development software, it takes more staff to create, transfer, and maintain test plans.

Using it for production e-test sacrifices throughput for the promise of additional coverage that is almost impossible to achieve.

- RF capability in this system slows down throughput and dramatically reduces accuracy of dc measurements.
- Despite marketing specifications touting 1fA and 1fF, guaranteed performance is much worse. Furthermore, probing parasitics overwhelm real device values at fA and fF levels.

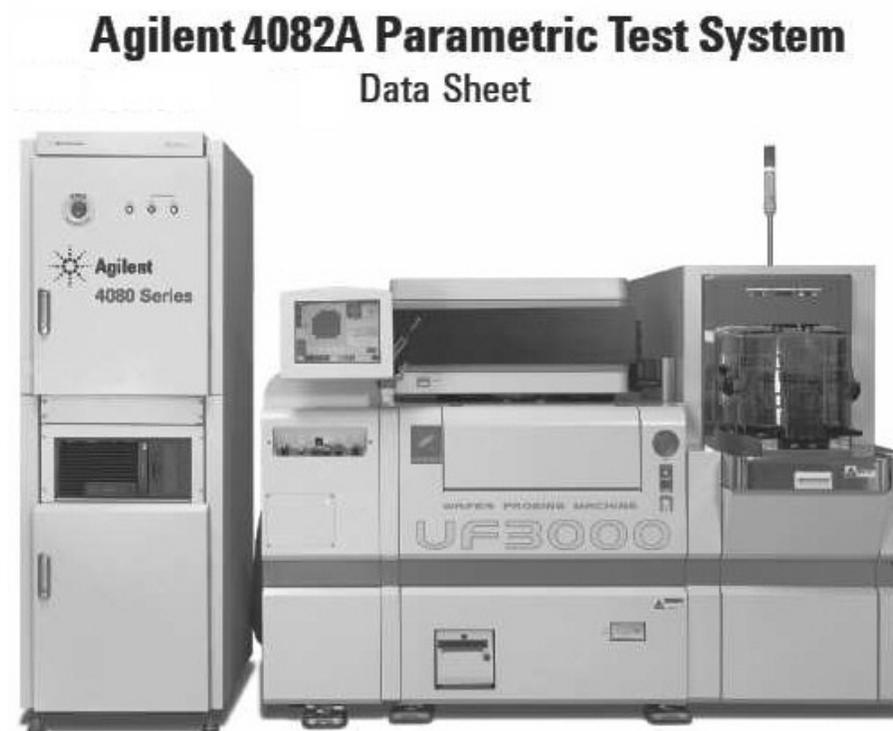


Figure 1 - Latest Agilent Development System

Look Closely at Specs

The chart below is from the 4082A spec sheet on the Agilent WEB site. Note that performance guarantees are 250 to 1000 greater than promoted resolution.

**Agilent 4082A Parametric Test System
Data Sheet**

General Marketing Description	Performance Specifications															
<p>DC Measurements Spot, Sweep, Pulse Bias, and Pulse Sweep.</p> <p>Measurement unit: HRSMU (High Resolution SMU),¹ MPSMU (Medium Power SMU and HPSMU (High Power SMU)</p> <p>Measurement range: 1 fA² to 100 mA, 2 μV to 100 V (using the two low current SMU ports) 10 fA to 1 A³, 2 μV to 200 V³ (using the 6 standard SMU ports)</p> <p>¹ Can be used only with ultra-low current matrix cards ² Using HRSMU. Using MPSMU, 10 fA to 100 mA, 2 μV to 100 V ³ Using optional HPSMU. Using MPSMU, 10 fA to 100 mA, 2 μV to 100 V</p>	<p align="center">Voltage Source/Monitor Range, Resolution, and Accuracy using HRSMU</p> <table border="1" data-bbox="805 590 1208 709"> <thead> <tr> <th>Full Scale Voltage Range</th> <th>Measure Accuracy</th> <th>Force Accuracy</th> </tr> </thead> <tbody> <tr> <td>±2 V</td> <td>a: 0.02% b: 0.025% = 500μV c: Rmat × I_o</td> <td>a: 0.03% b: 0.035% = 700μV c: Rmat × I_o</td> </tr> </tbody> </table> <p align="center">Current Source/Monitor Range, Resolution, and Accuracy using HRSMU connected to SMU1 and SMU2 ports</p> <table border="1" data-bbox="867 827 1341 1024"> <thead> <tr> <th>Full Scale Current Range</th> <th>Force Accuracy</th> <th>Measure Accuracy</th> </tr> </thead> <tbody> <tr> <td>±100 pA</td> <td>a: 4 % b: 0.4 + 0.0001 × V_o % c: 500 fA + 1 fA/V × V_o</td> <td>a: 4% b: 0.12 + 0.0001 × V_o % c: 500 fA + 1 fA/V × V_o</td> </tr> <tr> <td>±10 pA</td> <td>a: 4 % b: 4.0 + 0.0001 × V_o % c: 500 fA + 1 fA/V × V_o</td> <td>a: 4% b: 1.0 + 0.0001 × V_o % c: 500 fA + 1 fA/V × V_o</td> </tr> </tbody> </table>	Full Scale Voltage Range	Measure Accuracy	Force Accuracy	±2 V	a: 0.02% b: 0.025% = 500μV c: Rmat × I _o	a: 0.03% b: 0.035% = 700μV c: Rmat × I _o	Full Scale Current Range	Force Accuracy	Measure Accuracy	±100 pA	a: 4 % b: 0.4 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o	a: 4% b: 0.12 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o	±10 pA	a: 4 % b: 4.0 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o	a: 4% b: 1.0 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o
Full Scale Voltage Range	Measure Accuracy	Force Accuracy														
±2 V	a: 0.02% b: 0.025% = 500μV c: Rmat × I _o	a: 0.03% b: 0.035% = 700μV c: Rmat × I _o														
Full Scale Current Range	Force Accuracy	Measure Accuracy														
±100 pA	a: 4 % b: 0.4 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o	a: 4% b: 0.12 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o														
±10 pA	a: 4 % b: 4.0 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o	a: 4% b: 1.0 + 0.0001 × V _o % c: 500 fA + 1 fA/V × V _o														
<p>Two Terminal Differential Voltage Measurements Measurement Unit: Agilent 3458A Measurement range: 0.1 μV to 100 V (only when using ultra-low-current matrix cards), or 1 μV to 100 V</p>	<p>DC Measurement Subsystem: Digital Volt Meter (Agilent 3458A) Voltage Measurement Range, Resolution, and Accuracy (at number of Power Line Cycles ≥1)</p> <table border="1" data-bbox="1032 1041 1360 1220"> <thead> <tr> <th>Full-Scale Voltage Range</th> <th>Resolution</th> <th>Accuracy (% of reading + volt)</th> </tr> </thead> <tbody> <tr> <td>0.1 V</td> <td>0.1 μV</td> <td>0.01% + 100 μV</td> </tr> <tr> <td>1 V</td> <td>1 μV</td> <td>0.01% + 100 μV</td> </tr> <tr> <td>10 V</td> <td>10 μV</td> <td>0.01% + 200 μV</td> </tr> <tr> <td>100 V</td> <td>100 μV</td> <td>0.02% + 1 mV</td> </tr> </tbody> </table>	Full-Scale Voltage Range	Resolution	Accuracy (% of reading + volt)	0.1 V	0.1 μV	0.01% + 100 μV	1 V	1 μV	0.01% + 100 μV	10 V	10 μV	0.01% + 200 μV	100 V	100 μV	0.02% + 1 mV
Full-Scale Voltage Range	Resolution	Accuracy (% of reading + volt)														
0.1 V	0.1 μV	0.01% + 100 μV														
1 V	1 μV	0.01% + 100 μV														
10 V	10 μV	0.01% + 200 μV														
100 V	100 μV	0.02% + 1 mV														

Figure 2 - 4082A Specification Sheet with Comments

Current Guarantees are 500 Times Worse Than Marketing Hype

Resolution of 1fA touted in the general marketing description becomes 500fA for guaranteed performance specifications, and that is before effects of output voltage and voltage range are figured into the calculation. However, currents down to 500fA can be achieved in a production environment without undue care, and does not require adding extra costs to a \$300k prober to reduce chuck noise.

Low Noise Chucks are Needless Expense

For good low current measurements in a production environment, all that is needed is a probe card that guards against effects of dielectric absorption and measurements on the top of the wafer. Expensive probers with special low-noise chucks are not needed.

Test structures are simple devices, so they can be biased in such a way that measurements never have to be made with the chuck connected to a measurement node. Furthermore, test structures that require connection to the chuck should be redesigned to maximize measurement performance.

Chuck Current is not a Process Parameter

If test structures require measurement of chuck current, the test is not suitable for process control because factors influencing measurement quality easily overwhelm the measurement being made. In effect, the ability of the system to measure chuck current is being monitored, not the device.

Voltage Guarantees are 1000 Times Worse Than Marketing Hype

Voltage resolution of the system voltmeter is touted at 100nV, but guaranteed performance in the system is 100 μ V, or 1000 times worse. Even the more modest SMU resolution of 2 μ V is only warranted to 500 μ V while in the system. However, thermal emf's from dissimilar metals in the system can easily be >100 μ V, and copper to doped silicon is >300 μ V, so being unable to assure sensitivity less than the guarantee of 500 μ V probably does not matter. Additionally, software zeroing can compensate for steady state offsets.

Capacitance Guarantee at 100kHz is 150fF Compared to 1fF Marketing Hype

Low-level capacitance measurements are easily overwhelmed by the probing environment and by the test structure itself. Probe pad capacitance is such a limiting factor that capacitance assurance <1pF requires use of dummy pads for offset compensation.

The Agilent guarantee of 150fF is reasonable, but achieving 1fF uncertainty would require magic, even in a laboratory system.

Chapter 4

Using Reedholm Testers in Production E-Test

Variety of Cabinets - Same Instrumentation

Reedholm systems are not layered with frills or driven by planned obsolescence. That means they cost less and deliver all of the performance required for production applications. Some customers have termed their change to Reedholm as a retroactive, "Back to the Future" implementation where production e-test is kept simple and fast.

A variety of cabinets can house the highly modular Reedholm instruments shown in figures 3 to 5. The minimum footprint achieved by housing the instruments in the RI-EG high prober table below provides fast, cost effective operation for up to 6" wafers. For larger wafers, RI-40 or RI-75 cabinets are used. Really high pin count systems are put into the 7', RI-70 cabinet.



Figure 3 - Multiple RI-40's for 200mm Wafers



Figure 4 - RI-EG for 150mm & Smaller Wafers



Figure 5 - RI-70 Cabinet for Up to 600 Pins

Eliminate Risk of Obsolete Test Platforms

Within a few months, Keithley will stop providing support for the S400 testers. Support for previous models was dropped long ago. When Keithley support finishes, customers will have to arrange for spare hardware or repair by third party suppliers to minimize downtime. However, third party support has yet to surface. Agilent dropped support for the 4060 family many years ago, but some users countered by buying up used systems. Now Agilent is pushing customers from the 4070 family to the 4080 models.

Capabilities Were Not Driven by the Application

New Keithley and Agilent parametric testers were not driven by production e-test needs. If they had been, customers would not be able to run several generations of test systems side-by-side. But they can, and do. The test and measurement strategy of layering on new functions every few years, regardless of customer needs, was an expensive race that Keithley could not win, or handle, so they quit.

Continual Improvement Through Software

Production e-test is best served by test systems that do the job, not by having to purchase marketing inventions. Measurements have been largely unchanged for 30 years, but more powerful computers and continual software improvements dramatically improve productivity.

Bring Production E-Test Under Control

A veteran parametric test engineer got a laugh out of being asked about configuration control for Keithley parametric test software written by his company. When asked how there could be none in a production environment with all sorts of rigorous controls, he said that no one talked about it. Then he offered that relying on the judgment of parametric test engineers has not harmed his company. Maybe not, but how could that be, and why take the risk?

Use Standardized Test Algorithms from Reedholm

When new code is installed, improvements in Reedholm test algorithms are applied to all test plans. No edits are needed. Algorithms are modified through Engineering Change Requests (ECR's), so control over them is extended to the customer through formal software releases. Standardized algorithms are not a problem when production e-test is based on getting the right answer. When results change between old and new software, it means that test conditions were not as well characterized as previously thought and need to be fixed.

Configuration Control Over Test Conditions, Limits, and Coverage

Configuration control features in Reedholm RDS Intranet software assure that test parameters and test limits are under revision control at the customer site. Control over input conditions is through release of tests in the RDS Intranet database. In addition, test site hierarchy (tests > intradie test list > intradie pattern > die pattern) can be independently released because their content is not affected by the test content.

When a new test, test list, or test pattern is released, it is automatically used when the next lot is tested. There is no need to go to any of individual test system to effect the changes.

Define Process Testing and Restrict Testing to Them

By taking control of production e-test, manufacturing management can insist that all tests produce actionable data. That is, failures should point to a process step, or process step interactions. On the other hand, if results are within pass/fail limits, data should be trusted. That is, yield investigations should not look into parametric test results until all other possibilities are explored. When technology development releases test plans to production, tests that are not process specific need to be fully justified to management.

Test All Wafers in All Quadrants

Adaptive and parallel testing are band-aids applied to the real problem of inadequate speed and excessive testing. Testing multiple sites (5 for 150mm, 9 for 200mm, 17 for 300mm) and every wafer should not be a problem if care is taken setting up test plans. In an era of individual wafer processing, statistical sampling cannot find or prevent zero yield wafers or low yield zones on otherwise good wafers.

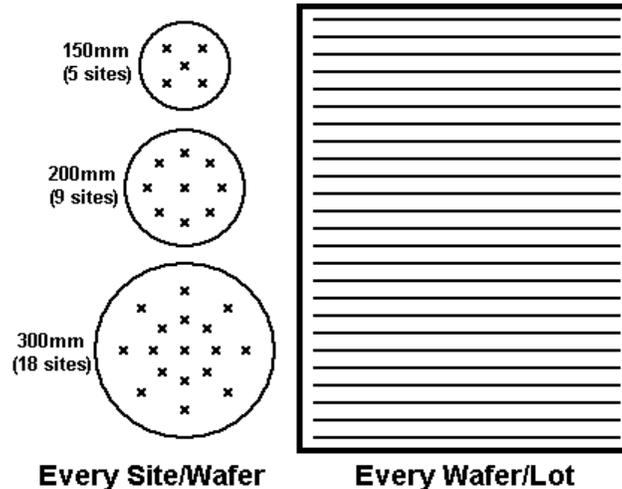


Figure 6 - 100% Coverage of Each and Every Wafer

Use Less Floor Space

The best way to free up floor space is to buy fewer testers. A formal hand-off of optimized test plans from development to production is a good start. Fewer testers are needed when production e-test is kept simple. By avoiding development testers with frivolous features, exotic and slow tests do not creep in.

When multiple obsolete testers are replaced, or instead of buying new Agilent systems, Reedholm speed advantages can free up >50% of the presently allocated space. Since test systems are kept in controlled environment clean rooms, saving a few square feet of floor space can add up to a considerable amount in only a few years.

Increase Productivity

Reedholm customers do not have to double-up on staffing for device engineering and programming. That is, a product engineer with device expertise does not have to be paired with

a programmer to get the job done. Once trained on Reedholm software, the engineer should be able to transfer new products into production in a couple of days. The rest of a product engineer's time can be spent improving yield or making yield information more available. For Reedholm customers, sustaining engineering for production e-test is a part time effort.

Stories from a Few Satisfied Customers

GaAs Foundry Reduced PCM Test Times by 7:1

Based on previous experience with Reedholm, a new operations manager included Reedholm when replacements for obsolete HP testers were evaluated. The evaluation justified the manager's confidence, and two testers were ordered for production. In addition to providing full coverage of test types, speeds with the Reedholm systems were so much faster that the complicated adaptive testing strategy written by the customer for the HP systems was scrapped. Now data is gathered from multiple sites across each and every wafer. Thus, going with Reedholm had the unforeseen benefit of getting back to 100% coverage. In addition to improving coverage, some previous measurement errors were corrected. For example, an uncompensated error of 30% in measurement of a parallel plate capacitor at 1MHz was identified by measuring at 100kHz.

SiC Depletion FET Test Times Reduced by 2:1

SiC FET testing was being done on a Keithley S400 using source code written by the in-house Keithley parametric test engineer. The group manager was not so sure that the code had to be unique, but the internal customer thought so as did the parametric test engineer. Reedholm was able to do the entire suite of tests using standard menu selections, and test times were reduced by 2:1. Furthermore, a channel pinch-off test that had been measured for years at $\sim 5\mu\text{A}$ was found to be 1000 times lower. In fact, it was less than the probe card noise pick-up of 2nA peak-to-peak. The incorrect value had not been found because the S400 did not have software tools to easily find that the current previously measured was from the drain to the substrate instead of through the channel.

GaAs Integrated Device Manufacturer Replaced Five Testers with Two RI-EG's

A valiant attempt to use an Agilent DC + RF system instead of obsolete Agilent dc only systems plus an RF station was not successful despite Agilent claims. RF calibration took so much time that DC test became a severe bottleneck. Shortly after they were installed, two Reedholm RI-EG systems were able to do the testing of four Agilent systems. The Agilent DC + RF station is now used solely for RF testing and device modeling.

Silicon Fab/Foundry Replaced Four Testers with RI-75 + Spare

An unmet need for 1500V testing on 150mm wafers was met with an RI-75 system. The RI-EG cabinet was not realistic because the customer wanted to use another type of prober for the application. The customer was pleasantly surprised to find that one RI-75 was able to do all of the testing previously done by four obsolete Agilent testers, thus freeing up the second RI-75 for engineering projects and development transfers.

Chapter 5

Reedholm Production E-Test System Features

The block diagram of a production e-test system configured for an RI-EG cabinet is shown below. This system can be expanded to more device pins and have additional test capability.

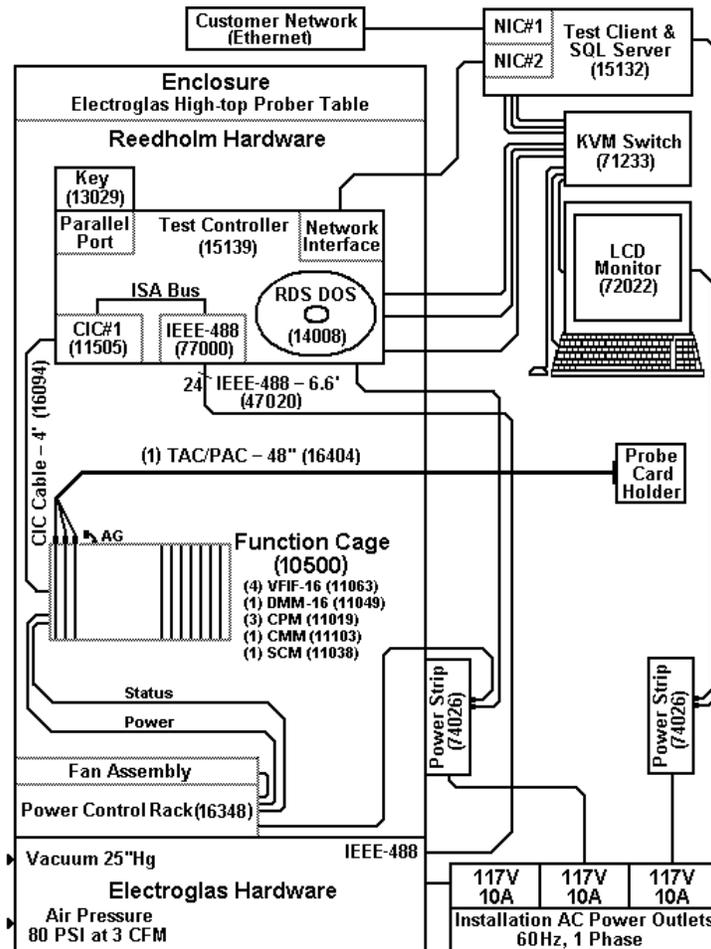


Figure 7 - RI-EG Intranet Configuration

Typical 24-Pin Configuration

- 24 Matrix pins.
- TAC/PAC interface to rectangular probe card that is easily adapted for circular cards.
- Force/measure currents from 100pA to 550mA with resolution of 3pA.
- Force/measure voltages from 50μV to 200V with resolution of 8μV.
- Capacitance at 100kHz from 100fF to 10nF with resolution of 3fF.

Enhancements

For slightly more expense, these optional capabilities can be installed:

- Sub-pA matrix that increases span to 100fA with resolution of 3fA.
- High current SMU for pulsing power devices to 5A.
- 2kV supply for breakdown measurements or characterization.
- Four channel pulse generation to confirm NVM cell operation.

Data Driven Software

The Reedholm graphical user interface is actually a WEB page, so it provides an intuitive interface that is easy to support through computer evolution.

- Delays and averaging are input directly as data records. There is no source code to hide excessive delays.
- Test algorithms are tightly controlled by Reedholm, but fully documented with on-line help.
- A rich set of inputs and outputs per algorithm assures coverage of test needs. With >20 years continuous evolution of process tests, there is little chance that standard routines cannot gather all required data.
- In keeping with the belief that there is one right answer, product and other device engineers have immediate access to optimization and characterization tools.

No Obsolescence – Timeless Systems

Unlike Agilent systems, Reedholm testers shipped in 1986 have been kept current through software and hardware updates. Computers have gone through several phases, and software has kept pace. Because continual improvement of software often highlights instrumentation shortcomings, changes to instrument modules are identified and incorporated when modules are sent to Reedholm for checkout or repair. With modest upkeep, the oldest instruments perform at essentially the same level as new ones. Customers do not have to concern themselves that two systems with instrumentation manufactured at different times might perform differently.

Device Test Oriented Software

Users do not have to be programmers or computer gurus to control test plans and data generated by Reedholm systems. Being able to explain transistor and resistor operation from I-V curves, or to explain semiconductor capacitance from a C-V curve, is adequate knowledge and background to be an effective user.

Rich Set of Input and Output Terms

Typically, one Reedholm test algorithm generates several parameters, and that algorithm has many input variables and output terms. That is not surprising since Reedholm has been improving the data driven test code for >20 years.

Example: V_t at Point of Maximum Slope

The routine that finds the point of maximum slope (PMS) outputs six parameters, has a rich set of input conditions, does extensive error checking, and computes output parameters.

Output Parameters

- 1) G_m extrapolated from PMS
- 2) V_t extrapolated from PMS
- 3) V_{gs} at PMS
- 4) I_{ds} at PMS
- 5) V_{gs} necessary for conduction to start the search
- 6) V_{ds} bias used during the test

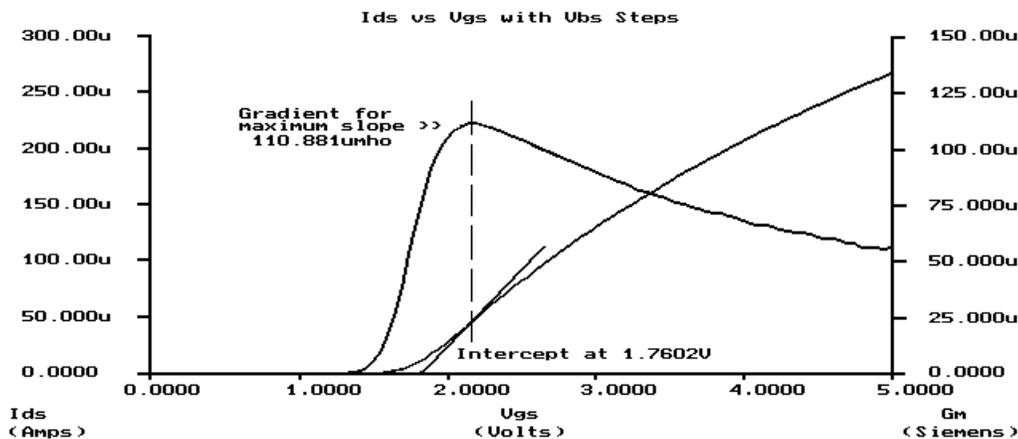


Figure 8 - Gradient (Slope) Overlaid on V_{gs} Transfer Curve

A rich set of test conditions can be input:

- 1) Five possible terminals: well, bulk, source, drain, and gate.
- 2) Up to 12 separate pins per device terminal.
- 3) Unassigned pins can be grounded.
- 4) Bias conditions for each supply, including current limit value.
- 5) Span of V_{gs} for search.
- 6) Delays for settling after initial bias and after each step.
- 7) Whether to use AC power line synchronous averaging.
- 8) The number of readings to be averaged for noise reduction.

Each test can be used for dispositioning:

- 1) Three double-sided sets of limits are available for each test.
- 2) Each test can be used for continuity and for wafer lot dispositioning.
- 3) Error conditions encountered during testing, e.g., a voltage-forcing supply in current limit, select a numerically assigned code that is multiplied by a very large multiplier ($1e+20$) to invalidate results. Also, fail codes are listed in the on-line help and link to pop-up text errors during test debugging.

Software Configuration Control

When new released code is applied, improvements in Reedholm test algorithms are used for all test plans without having to make any edits. Reedholm controls test algorithms through Engineering Change Requests (ECR's), so control over the test algorithm source code is at handled at Reedholm and extended to the customer.

Control over input conditions is through release of tests held in the RDS Intranet database. A master test table holds all tests, released as well as engineering ones. The hierarchy above a test can be independently released because their content is not affected by the test.

Operators are restricted to running released tests. Engineer and administrative privileges permit running test versions still under development at the same time as released tests. Separate test patterns do not have to be created.

In other words, production can run a released version when engineering does not tie up the tester running an evaluation version.

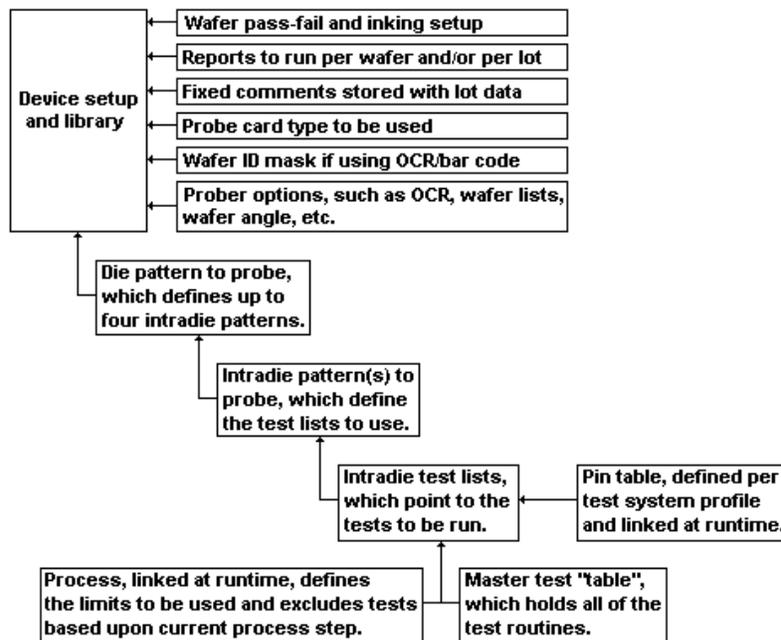


Figure 9 - Reedholm Test Control Hierarchy

Memory Mapped I/O Control

Modular instruments plug into an analog/digital back plane without slot dependence. That is, any module can go into any slot as long as the cabling that connects the instrument to the outside world can reach it. Manual DIP switches set each address. Most modules contain 64 bits of address space that hold instrumentation control information, measurements, and Boolean flags.

Menu-driven troubleshooting software allows investigation of the instrumentation status at any time as shown the figure 10 memory map. In the map, cross Point Matrix (CPM) #1 is at 00h, #2 is at 08h, etc. Each hexadecimal address location shows the contents of one byte in hex code. The 256 locations shown in the map contain 2048 bits of data.

```

*****
Instrumentation Memory Map:  MemBase =      Group = 0
*****
2nd Adx Char --->  0 1 2 3 4 5 6 7   8 9 A B C D E F
1st Adx Char -> 0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 1  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 2  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 3  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 4  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 5  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
1st Adx Char -> 6  48 01 7F F7 10 02 FF 00 20 01 7F F7 10 02 FF 00
1st Adx Char -> 7  4C 01 7F F7 10 02 FF 00 5F 01 7F F7 04 00 00 00
1st Adx Char -> 8  00 29 7D 00 00 00 01 00 00 42 00 00 20 00 01 00
1st Adx Char -> 9  00 18 00 00 00 00 00 00 73 21 7F FF 00 5C 6C 00
1st Adx Char -> A  50 54 45 54 2E 4F 38 00 00 00 00 00 00 00 00 00
1st Adx Char -> B  38 04 7F F7 10 00 00 00 57 04 7F FF 04 00 00 00
1st Adx Char -> C  00 84 00 00 00 00 00 00 00 84 00 00 00 00 00 00
1st Adx Char -> D  00 84 00 00 00 00 00 00 00 84 00 00 00 00 00 00
1st Adx Char -> E  00 00 00 00 00 00 00 00 00 7F FF 00 00 00 03 30
1st Adx Char -> F  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 38

```

Figure 10 - Instrumentation Memory Map

There are no microprocessors or state machines to interfere with this flat hierarchy of direct instrument control. As a result, this approach provides excellent system characteristics:

- Maximum system control because all states can be directly controlled. Unlike other complex systems that can lose communications with controlling software, Reedholm instrumentation never gets in a state that one has to power down to regain control.
- Highest possible speed because each and every register can be directly read from, or written to, without going through a prior sequence.
- Detection and recovery from loss of control when high energy noise from voltage breakdown flows through the instrumentation. By reading the memory map before high voltage and breakdown tests, changes to the map are detected and the original value are restored in 500µsec, well before relays have a chance to change state. Thus, breakdown events are detected if missed by the measurement code.

On Demand Optimization Tools

Testing speed should be as fast as possible as long as accuracy is not compromised. So any system intended for production e-test needs to have software tools that allow a device engineer to prove that data is accurate and how long it takes to settle to a repeatable reading. As of this writing, Agilent does not provide this capability in a form that can be run easily by Agilent programmers, let alone by product and device engineers who provide device knowledge.

Reedholm provides current vs. voltage and capacitance vs. voltage plots that precisely show what the correct test results should be. For sensitive voltage and low current tests, it is particularly useful to take data as a function of time after stimulus is applied. Knowing how long it takes to get to the correct answer, individual tests as well as groups of tests are run to find result statistics and how long each test takes to execute.

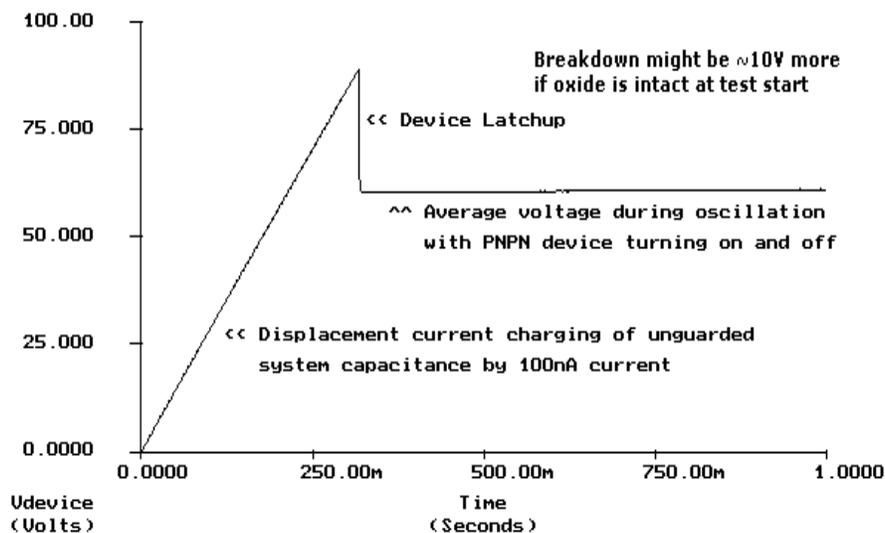


Figure 11 - Timing Output for PNP Latchup

Response Timing Plots

Timing plots are heavily used by Reedholm during software and instrumentation development as well as for applications troubleshooting. The figure above was generated while working with a customer to uncover peculiar system behavior after a breakdown test. What had seemed to be a fairly innocuous oxide breakdown test with 100nA forced into a gate had turned on a PNP device with one terminal being the backside of the wafer. In itself, that was not a problem, but the PNP device biased the chuck to >50V with no turn-off path when the latching condition was removed. Subsequent grounding of the chuck caused extremely high RF EMI that led to software aborts. Attempts to use an oscilloscope were thwarted when the probe discharged the chuck. Once the problem was identified, test conditions were used to control the chuck voltage.

Production Test Times

During production testing, execution time for each individual test is measured, but not stored. Instead, the average, minimum and maximum values are found and stored for each wafer lot.

Timing data can be displayed on the monitor or put into a lot report. Using that displayed or printed report, particularly slow tests can be identified for more careful examined in maximizing throughput.

Software Bottleneck is Eliminated

By providing tools that do not require programming or computer expertise beyond being able to navigate with WEB pages, a Reedholm implementation avoids the bottleneck caused by transferring technology development source code to production. All that is needed for Reedholm test plan set up and optimization is an understanding of the simple electronic devices in the PCM test structures. It isn't necessary to find the equivalent of an "Agilent engineer" to support Reedholm software or to introduce test plans to production. Any member of the technical staff with device knowledge can do the job, so it does not become a dead-end position or one that restricts development of new engineer hires.

Source Code Trap

In figure 12, the set of screens on the left for a code generating interface are similar to ones on the right that are from Reedholm software. But that is where the similarities end. The interface on the left spawns source code while the Reedholm interface populates data base tables. Reedholm continual enhancement of the test engine has led to a set of input and output parameters far richer than provided by Agilent.

Of course, Agilent programmers can modify source code, and all do to some extent. That is why parametric testing with Agilent systems requires two people at the minimum: one to program and one to determine if results make sense. Linux and Unix operating systems require additional programming skills and manpower for effective use.

The resulting source code is almost impossible to control, but that is not surprising since the starting Agilent code has no warranty about working right. If the low level commands do not work right, the Agilent warranty is limited to replacing the software media. Thus, Agilent does not fix algorithms that do not produce correct results—that is left to the customer.

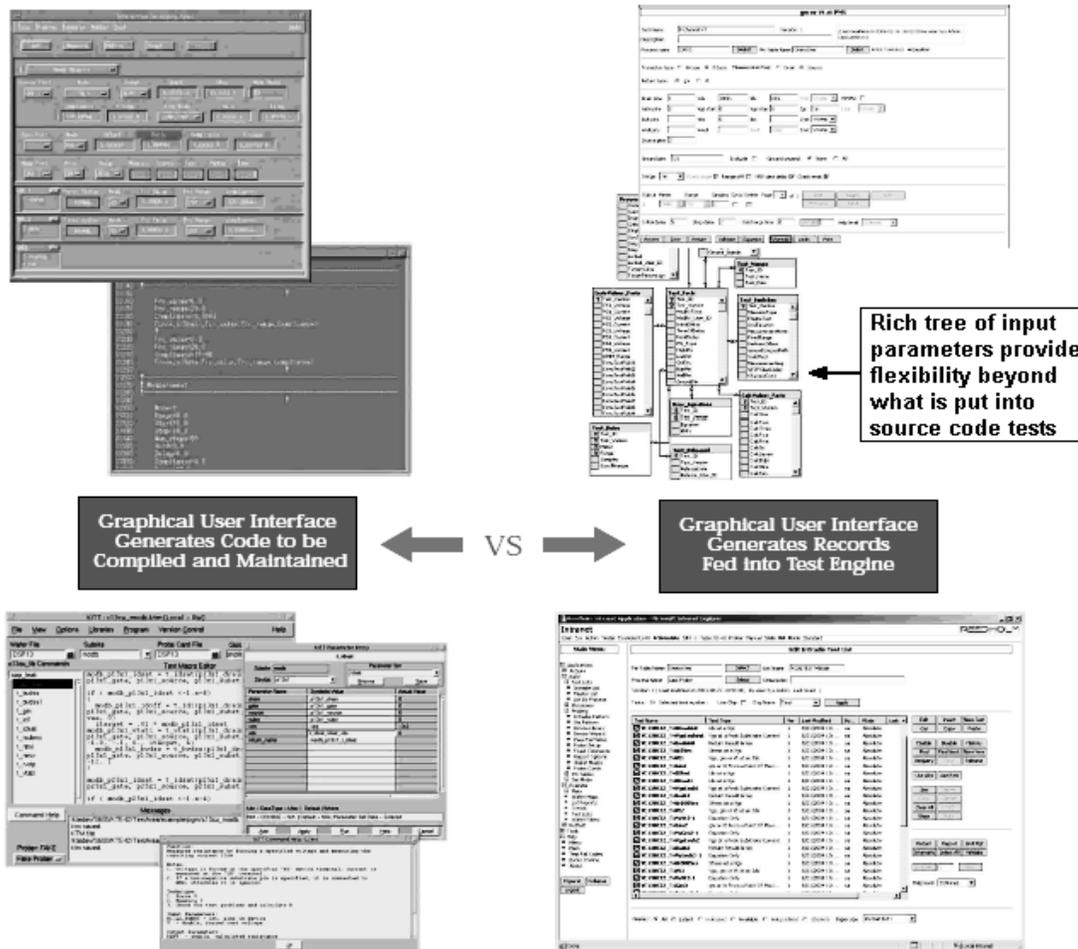


Figure 12 - Source Code is Different than Reedholm Data Driven Approach

No Magic to Parallel, or Multi-Task Testing

Contrary to the implications of the latest Agilent offering, process tests by themselves do not create a bottleneck in parametric testing. If the longest allowed test time is 100msec, and multi-threaded test software would lead to bottlenecks merely due to latency imposed by thread-handling.

While wafer level reliability might have many simple devices whose testing might benefit from parallel testing, that is seldom the case in process monitoring. For PCM testing, the most complex device on a sub-die has to have a set of dedicated instruments, and not much is left for other tests, if there was time to do them.

From the Agilent viewpoint, there is not much to lose if the touted advantages of multi-tasking test instruments and the test controller do not materialize. Resultant test plans will be so complex there will be little chance of optimizing before transferring testing to production, and more testers will be purchased than should be.

Chapter 6

Getting Started with Reedholm

Whether being used in a start-up company, at an expansion facility, or as replacement of an obsolete system, Reedholm seeks to have system requirements well defined before starting to build it. Following the build, Reedholm:

- Proves that the system meets the documented requirements before shipping.
- Confirms that requirements are still met during installation.
- Provides tools that assure the system continues to meet requirements—indefinitely.

No Risk Evaluation Using Tested Wafers

Changing to Reedholm systems from another production e-test implementation can improve throughput by several hundred percent if customers have made few efforts to eliminate needless or excessive delays, averaging, and autoranging. Before an order is placed, Reedholm can prove a speed advantage using customer wafers.

Flexible Algorithms Provide Full Coverage

Besides showing a speed advantage, an evaluation shows that standard Reedholm routines can gather all process related data. That means that the product engineer participating in the evaluation does not have to be a programmer—device knowledge is sufficient. In the unlikely chance that a routine is deficient or doesn't exist, Reedholm works with the customer to define a routine that will do the job.

Correlation to Correct Results

Previous results of parameters used in an evaluation are usually correct, so correlation with Reedholm results is easy to prove. However, there are cases in which data taken for years is wrong, and the right answer has to be found. Since the starting point for Reedholm is characterization of each test, discrepancies between previous data and Reedholm data happen early in the evaluation so the right answer is found immediately.

Implementation After Order Placement

If the evaluation justifies placing an order for a Reedholm system, and if the Reedholm system is going to replace or eventually supplant other systems, one or two engineers should be selected to be champions during the conversion to Reedholm testing. Programming skill is not needed as long as the technical people in charge of implementation have basic testing knowledge (i.e., understand force I, measure V relationships), can operate or interpret curve tracer software built into the RDS Intranet, and understand test structure devices.

Integrating Reedholm Database

While the system is being built, output reports and the work flow interface are documented in detail so that the Reedholm database can be integrated with customer requirements during the installation visit. If the customer does not have staff with SQL expertise available, Reedholm does the work for modest fees. The integration documentation is reviewed prior to training and finalized by the end of training at Reedholm.

Training on Reedholm Structures

Initial training in use of Reedholm test algorithms is done using simple IC's or devices soldered to DIP headers. These tough test structures allow errors to be made without destroying devices and provide attendees knowledge of the scope of Reedholm test software.

Reedholm strives to arrange testing on customer wafers to solidify training before shipment.

Assuring Operation on High Volume and Demanding Processes

When initial training is done, and before a system ships, the knowledge should be applied to test plans that span customer high volume and special processes. The quantity of test plans to be ready prior to shipment are negotiated prior to order placement. Since customer testing documentation is seldom complete or fully accurate, Reedholm cannot do this work independently. Those who attend training and stay for a week or two for test plan development have to be quite knowledgeable about the structures so that tests can be optimized, correlated, customized, and made ready for production release.

Installation

Installing and getting the system operational is fairly quick. Facility requirements are sent out shortly after order acknowledgement so that the customer can prepare ac power, air pressure, and vacuum lines for the test system and prober. Within a half-day, testing can usually be started to confirm data taken before shipment. Shortly after that, wafer level results can be correlated with results from other test systems.

Correlation of Test Plans

Test plans generated at Reedholm before shipment are run at the customer site to show that results correlate with those gathered before shipment. Discrepancies are addressed by finding out what the right answers are, determining why there were differences, and finding out how to always get the right answers.

Integrate with Work Flow

With person responsible for customer IT, the test system is integrated into the customer network. If Reedholm was contracted to modify or create hard copy or electronic reports, that work is confirmed after test results have been correlated.

Continual Improvement

Once new systems are installed and operational, Reedholm provides support for continually improving the production e-test operation.

Systems of Spares for Engineering Investigations and Technology Transfers

In the rare event of module failures, spares need to be on-hand to minimize downtime. Even if there are multiple Reedholm systems at a site, the best place to keep spares is in a system that is kept running at all times. When not being used, Reedholm self-test software should be used to loop indefinitely and thus assure that all of the assemblies in the system are ready for replacement in production systems if there are problems.

Technology Transfers

Besides being a source of spares, the prime purpose of such a system is to transfer new products to production. Prior to formal hand-off from development to production, the system is used to optimize test plans for speed and accuracy. A manual prober is adequate for technology transfers,

Yield Investigations

A secondary use of a system of spares is yield troubleshooting. Instead of taking time away from production testing, an automatic prober hooked to the system would make it possible to do yield investigations when the problem does not reveal itself at every PCM site.

Remote Sessions

Modern software such as GoToMyPC make it practical for support engineers at Reedholm to directly participate in system troubleshooting as well as investigation of device measurement problems. This type of software requires that the customer open a port completely under the customer control. In addition, the port is only open for a specified period of time during which Reedholm has access.

Remote support is provided at no charge as long as sessions are reasonably short and do not unfairly tie up Reedholm personnel.

Changes Driven by Customer Inputs

Reedholm software and hardware changes are made under an engineering control system driven by customer problem reports and software feature requests. Engineering change request (ECR) numbers are issued as soon as they are understood well enough to be fully specified or duplicated. After changes are complete, information about them is posted on the Reedholm WEB site. The result is continually evolving software.

Changes are bundled into software upgrades every year, or whenever it is more convenient for Reedholm to provide an upgrade than to direct the application of patches that address deficiencies that interfere with use of the software.