SUPPORT NOTE

SN-114

Power Down Protection for Sensitive EM Structures

Introduction

Effective power down software in an automatic test system must protect the device under test (DUT) without causing damage to the instrumentation being used, but cannot do so without regard to test speed.

Controlled power down methods were used in the first version of Reedholm data driven software and have been continually refined. Such code is called at the end of every test with the intention of returning the test environment to an initialized state without causing device damage. This is particularly important in protecting very fast devices with low tolerance for the inductive voltage spikes that can occur when current is suddenly interrupted. Wide use of Reedholm systems at GaAs wafer fabrication facilities demonstrates the effectiveness of Reedholm power down methods.

Recently, a situation was encountered that led to a significant improvement in the power down code that prevents charging of the DUT cable and interface after removing power from very low resistance test structures. This improvement did not require alteration of the code that prevents damage from inductive kickback to GaAs and other high mobility devices.

Charging Considerations

To an adequate approximation, the time it takes to charge a capacitance to the desired voltage is inversely proportional to the driving current and proportional to the capacitance. There are two dominant factors in estimating systemic capacitance that might be loading a power supply, or supplies, in a Reedholm system.

1) With a typical instrument configuration, nodal capacitance is ~300pF. That is the minimum capacitance load that a device pin, or two instruments connected without a pin, will have.
2) Each device pin attached to a node increases the capacitance by ~20pF.

Those capacitance levels are inconsequential since a test current of 1mA would discharge a 320pF capacitor charged to 10V in 3.2µsec, or much faster than the switching elements used in high quality parametric test systems. For instance, it takes the dry reed relay switches used in Reedholm systems from 400µsec to 800µsec to open and 600µsec to 1100µsec to close after receiving a command to do so.

Previous Power Down Algorithm

Before the improvement documented in this note, to assure transistor protection sources were powered down in a controlled sequence followed by a delay that was sufficient to reach 0V before any instruments or device pins were disconnected. Furthermore, the delay was increased if the limit bits associated with a source (Vzero indicating <±360mV and NOT Ilimit indicating that the source voltage was under control). At that voltage level, relay hot switching is avoided, and residual charge left on systemic capacitances is insignificant.

The deficiency of this previous algorithm was difficult to assess because it seemed obvious that such a strategy had to work and because the conditions that led to problems were highly situational. That is, one had to deliberately select components or disable circuit elements in order to investigate the problem that was first only seen using a high-speed storage oscilloscope at the reporting customer's site.

Problem Review

Executing a series of 4-Terminal Resistance measurements tended to cause occasional shifts in some of the resistance values. Residual charge that was left on the wafer DUT wiring as the result of measuring a device was suspected of causing damage to the next device that was measured. This occurred in spite of the existing power down procedure. However, the problem happened intermittently and sometimes months would pass before it was seen again.

Postulated Damage Scenario

The EMPAC test grid for 4-Terminal Resistance is shown in Figure 1 with the corresponding circuit diagram in Figure 2. The bubble pairs represent the relay switches that connect the instruments or matrix pins (P3, P4, etc.) to the system nodes (N0, N1, etc.).

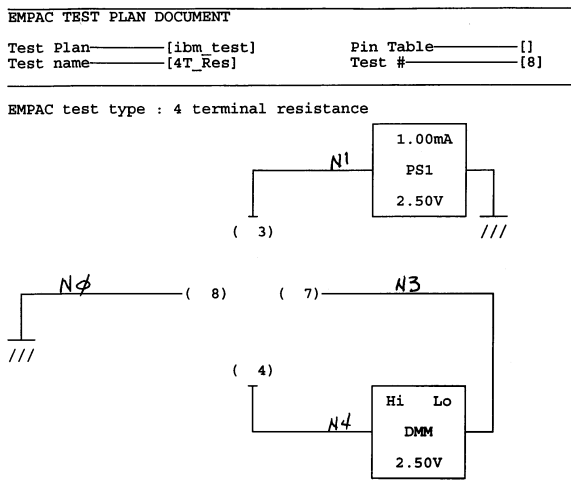

Figure 1

From Figure 2, one can postulate that the only way that residual charge can be left on the nodes is if a) PS1 is not at zero volts, and b) the low-side load connection opens before the high-side load connection opens. This means that the low-side connection relay for P8 would have to open before the high-side connection of PS1 to N1 or the high-side connection of P3. Depending upon the relative relay opening times, this circumstance might allow PS1 to charge the stray capacitance of N1, N3, N4, and the pin wiring for P3, P4, P7, and P8.

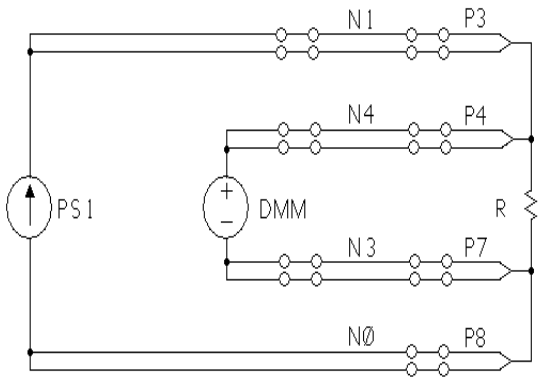

Figure 2

Emulation Test Vehicle

To test the postulated damage scenario, a particular pair of pins that meets the timing requirement must be found: a pin to use for the high-side connection that opens substantially later than the pin used for the low-side connection. Such a pin pair, reflected in Figure 1, was found for a particular CPM with a 200µs difference in opening time.

Having the proper timing relationship between the high and low pins, the postulated damage scenario could now be tested by monitoring the voltage across the DUT while running a two-loop test. A 100Ω resistor was used to emulate the problem device. If the problem had occurred, it should have been observable as a spike of energy across the DUT at the beginning of the second test. What was seen is shown in Figure 3, with a time-expanded version is shown in Figure 4.

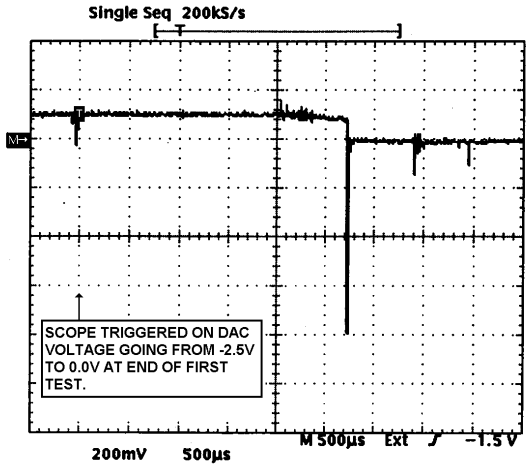

Figure 3

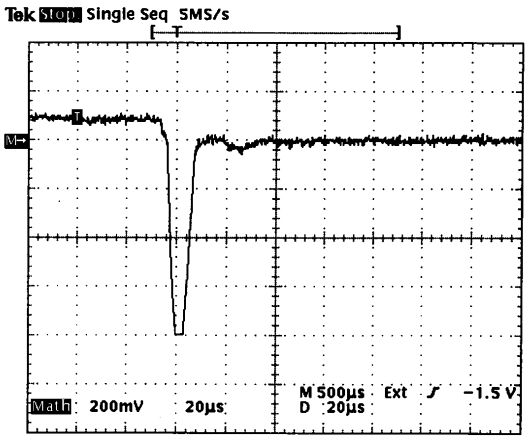

Figure 4

Thus, having carefully chosen a pair of pins, it was possible to demonstrate a source that potentially has enough energy to damage a DUT. Additionally, and more importantly, there was now a test vehicle that could be used to show such an energy spike every time the two-loop test was run. Thus, it was used to verify possible solutions.

Circuit Status During Test

When a VFIF is in current limit, the voltage control loop is open. Referring to Figure 5, this means that the following conditions apply:

- Voltage DAC is set to –2.5V (determined by test grid of Figure 1).
- Voltage across 4.7nF cap is about 700mV due to voltage limiting feedback (not shown in Figure 5).
- Vin (TP 12) is about 14V.
- Voltage Clamp limits output of VCCS to 1mA (determined by test grid of Figure 1).
- Output voltage is 100mV for a 100Ω load.

The Vzero bit is true when the output voltage magnitude is less than 360mV, and the Ilimit bit is true when the voltage at TP 12 is greater than 10V.

Applying these definitions to the conditions that exist during the test, one can say that both the Vzero bit and Ilimit bit are true. Although it could be said that the Vzero bit is giving an incorrect indication in that the output voltage is not zero, one could expect that the delay algorithm should produce the necessary delay on the basis of waiting only for the Ilimit bit to go false.

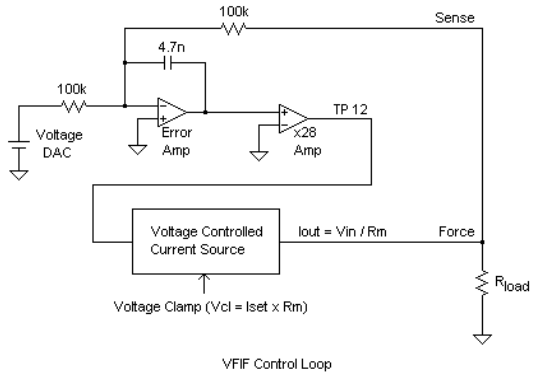

Figure 5

Explanation of Spike

In order to investigate possible causes of the voltage spike, the voltage at TP 12 in Figure 5 and the voltage at Node 1 were monitored from the point at which the power down procedure is invoked and the point at which the instrumentation is connected for the following test. This is shown in Figure 6 where the scope is triggered on the DAC voltage going to 0.0V from –2.5V.

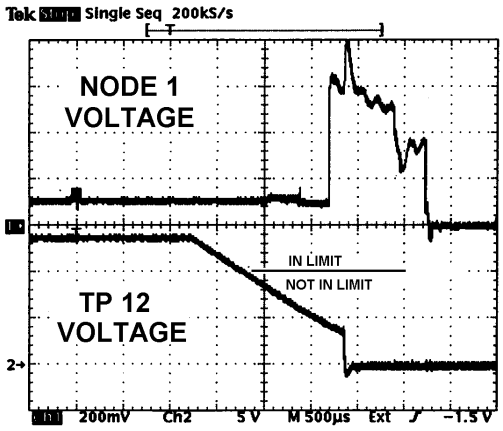

Figure 6

Observations from Figure 6 follow:

- The trigger occurs 500µsec from the left edge.
- The VFIF takes 1.7msec to get out of current limit after the DAC is set to 0V (trigger).
- Node 1 is charged to >600mV at disconnect.
- The VFIF is not at 0V at disconnect.
- The VFIF is commanded to connect for the next test ~3.4msec after the trigger.
- The VFIF actually connects ~3.7ms after the trigger, discharging the node to 0V.

In summary, Figure 6 shows that the existing power down procedure fails to meet its objectives. That is, the output voltage is not zero at disconnect time.

This can be explained by further consideration of Figure 6. Note that the voltage at TP 12 changes relatively slowly as the control loop transitions from the current limit state to the voltage control state. When the current limit bit goes false at 1.7ms after the trigger, the software delay loop is terminated and the command to disconnect pins and instruments is asserted. The pins are disconnected first, followed by the instruments. It is clear from Figure 6 that the low side of the load disconnects about 2.7ms after the trigger because the Node 1 voltage starts to increase at that point. The VFIF actually disconnects at approximately 2.9ms after the trigger because it is at this point that the voltage moves quickly to zero.

It is also worth mentioning that if the output voltage had reached zero between the time that the current limit bit went false (1.7ms) and the time that the low side of the load disconnected, some 700µs later, residual charge would have been nonexistent. This explains why the problem occurs only for low values of load resistance, for it is the output voltage that determines the speed at which the amplifier can restore itself to the voltage control mode.

Referring again to Figure 5, the 4.7nF feedback capacitor around the Error Amp must be discharged from 700mV to 0V. The current that is available to accomplish this flows through the 100kΩ resistor connected to the output. Therefore, the lower the load resistance at a given current limit, the lower will be the output voltage. The lower the output voltage, the slower the voltage across the capacitor will be restored to ~0V as can be seen in the following equations.

$dt = CdV/I = (4.7nF)(700mV)/(Vout/100k\Omega)$

$dt = (4.7nF)(700mV)/(100mV/100k\Omega) = 3.3ms$

Using the above equation and Figure 6, we can predict that if the load resistance had been 200Ω instead of 100Ω, the amplifier recovery time would have been about 1.65msec (twice as fast), and there would not have been a residual charge problem.

Modified Power Down Procedure

In addition to addressing the known problem, the new algorithm needed to continue to meet the general design objectives. To fully discharge the DUT, for example, all system pins are grounded as part of the revised procedure. It was also very clear that reliance on the digital bits Vzero and Ilimit was inadequate.

An algorithm that satisfies all design requirements is shown in the timeline of Figure 9. The following steps became part of the modified procedure:

- Calculate a delay time to slew to 0V based on the load capacitance and current limit setpoint.
- Delay until all sources are at 0V.
- Disconnect sources without current limit.
- Set sources with current limit to 0A.
- Disconnect sources with current limit.
- Delay until all sources are disconnected.
- Connect all nodes and pins to ground.
- Delay until all sources are disconnected.
- Restore the current limit settings for all sources.

The actual sequence of events is complicated by the latent period between when a relay is commanded and when it actually switches. In Figure 9, it is seen that the relay commands are appropriately interleaved with the resulting switching times so as to accomplish the objective without undue delay. With this new algorithm, reliance on digital indications of 0V and 0A has been eliminated.

Revised Circuit Status

The same setup that was used to obtain the information for Figure 6 was used to show how the software changes affected the waveforms. This is shown in Figure 7 from which we can observe the following.

- Trigger occurs 500µs from left edge.
- Current is set to 0A at 250µs after trigger.
- VFIF disconnect command is 300µs after trigger.
- VFIF disconnect occurs 850µs after trigger.
- Nodes and pins are grounded from 900µs to 1000µs after trigger.
- Node 1 disconnect occurs 1.4ms after trigger.
- Current setting is restored 1.6ms after trigger, and VFIF recovers quickly from current limit.
- Connect command for next test occurs 2.6ms after trigger.
- Actual connect occurs 3ms after trigger.

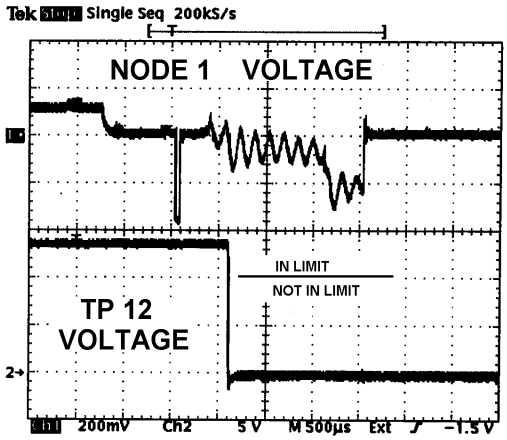

Figure 7

Most noteworthy is the fact that the voltage spike that was seen in Figure 3 and Figure 4 no longer exists. This can be seen in Figure 8, which is the voltage across the 100Ω load resistance.

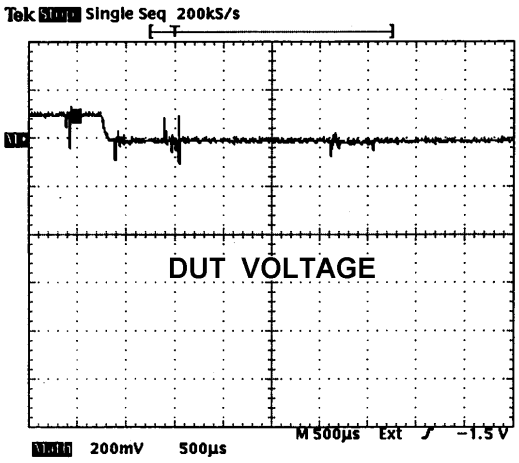

Figure 8

Conclusion

From the evidence, it is clear that the first two design objectives are met by the new algorithm. Instrumentation that supplies energy to the test environment is completely powered down. All DUT leads are fully discharged prior to being disconnected.

Additionally, the timeline of Figure 9 shows that test speed is maintained so that throughput is not affected. In fact, because the power down routine now grounds all matrix pins, no Discharge Time should need to be defined under the EMPAC Editing Options. When upgrading to RDS 8.01 or later software, test plans can be further optimized by eliminating this choice.

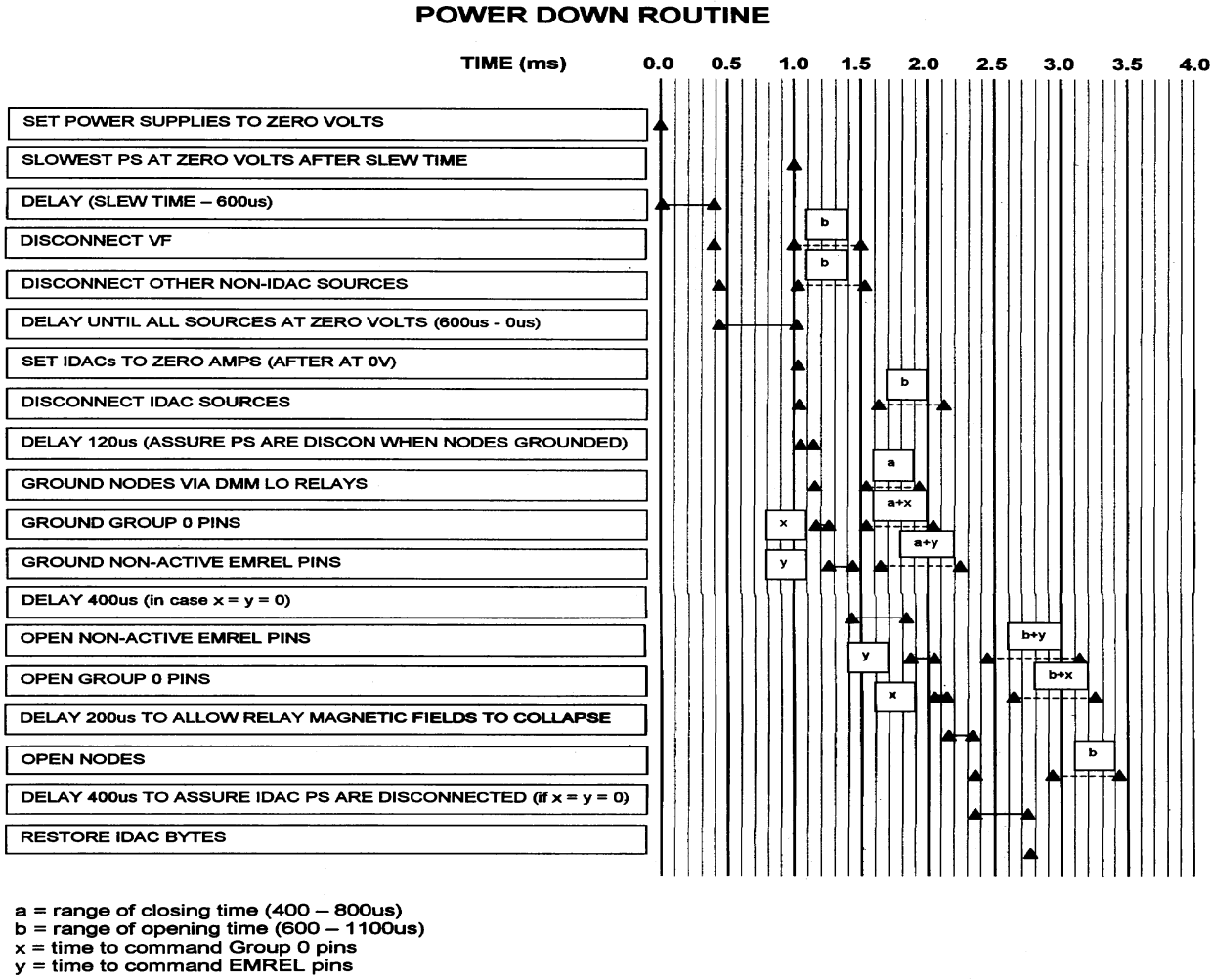

Figure 9- Timing Relationship During Power Down