SUPPORT NOTE

SN-119

Verification After Calibration

Introduction

Several levels of diagnostic checking are available via pull-down menu selection using the standard Reedholm software. These tests check the connection integrity of the switch matrix and instruments. In addition, they check the output voltage and output current of all sources relative to the measurement capability of the DMM. Additionally, accuracy can be enhanced through use of self-calibration software.

While the standard Reedholm verification software is comprehensive, it executes rapidly and without user interaction. As a result, sometimes questions are raised about additional verification. This note provides an overview of the standard Reedholm software and suggests a simple method to gain confidence that no additional verification can be justified.

Diagnostics

The Maintenance section of the System Manual contains a sub-section on Diagnostics showing the test choices available from the Diagnostics Menu. Failure limits for those tests are also described in the manual.

Standard diagnostic tests do a thorough job of verifying the quality of the system measurement, sourcing, switching, and cabling elements by showing that:

- Instruments are performing to specifications.
- Instruments can be connected to all system pins.
- No connection shorts exist.
- Connection resistances are not excessive.
- Voltage sources can deliver specified voltages.
- Current sources can deliver specified currents.
- Parasitic leakage currents are not excessive.

Enhanced Accuracy with SelfCal

In addition to the diagnostics software, Reedholm provides a Self Calibration Module (SCM) that permits tracing to an external standard. Use of this is covered in the calibration section of the system manual. An SCM provides stable reference voltages and currents for most dc instrumentation ranges. SCM reference values are measured by an external standard, typically a high resolution/high accuracy digital multimeter, to establish precise SCM values. Once the reference values are measured and stored, a menu-selectable test routine, SelfCal, is run to calculate correction constants for the DMM and all dc sources relative to the precise SCM values. Those correction constants are used when testing to maximize traceability to customer maintained or out-sourced standards.

Load Effects On Accuracy

Diagnostic testing with the loopback card assures delivery of proper currents and voltages to the probe card connector. Maximum output voltage and current are measured as part of that testing.

Because voltage accuracy and current delivery are measured during other tests, there is no reason to do that on the probe card. However, it is understandable that one might want to be reassured that full power signals can be delivered without loss in accuracy.

This can be accomplished using a resistor that has the required power capacity at the conditions of interest. Thus, if the maximum voltage of 100V were applied to a 500Ω resistor, the maximum current of 200mA would flow. Of course, the resistor would have to have a power rating of at least 20W.

An EMPAC 4T Voltage test can be used to measure an open circuit voltage and then repeat the test with a 500Ω load. Using the equation feature, the shift could be calculated and expressed as a percentage of the nominal voltage. If the system can pass diagnostics including the loopback test, any shift measured will be well within the specifications of the system.

EMPAC Test Setup

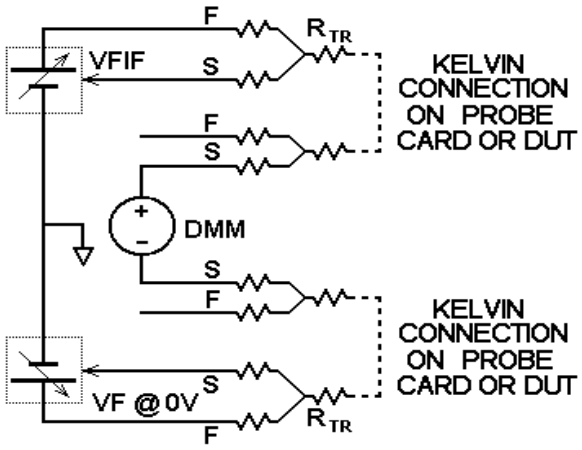

Figure 1 - Four-terminal EMPAC Test Without Load

Referring to Figure 1, the voltage measured by the DMM at the probe card will be exactly the same as that measured at the instrument backplane, even though there may be resistance associated with wiring and circuit board traces, because there is no current flow.

Referring to Figure 2, the voltage measured by the DMM at the probe card will be lower than the VFIF set point voltage because of the voltage drop across resistance R_{TR} in both the high and low force leads.

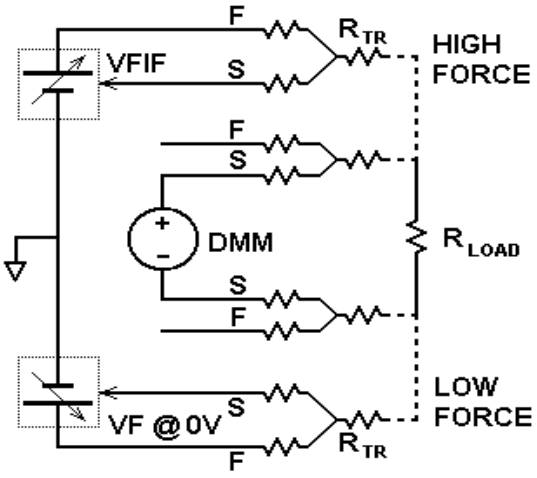

Figure 2 - Four-terminal EMPAC Test With Load

Components that comprise R_{TR} include all resistances on the load side of the point where the DMM is connected to the Force pins. This might include probe card trace resistance, probe contact resistance, and DUT Resistance. With careful consideration of how this connection is accomplished, resistance R_{TR} can be made virtually zero.

EMPAC Test Grid

A variation of the standard EMPAC Four-terminal Voltage test can be used to verify the voltage that is delivered at the probe card. The test grid is shown in Figure 3. Low side of the load is driven by PS4 in order to assure that the low-side voltage is virtually zero even in the presence of resistance in the low-side force connection. The test grid uses these pin assignments:

- High Force: Pin 1
- Low Force: Pin 10 (or any unused pin)
- High Sense: Pin 3
- Low Sense: Pin 4
- Bias Pin: Pin 2
- Bias Voltage: 0V
- Bias Current Limit: 200mA if VFIF is used.

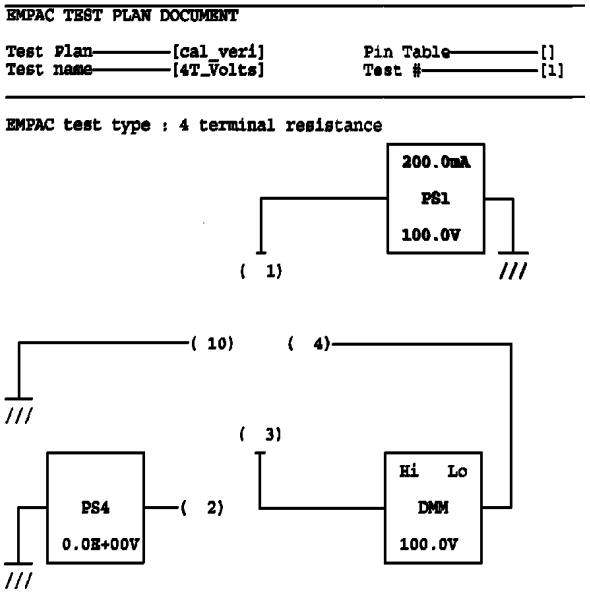

Figure 3 - EMPAC Test Plan