REEDHOLM

SUPPORT NOTE

SN-136

Test Structure Induced Hot Switching

Introduction

The switching sub-system is a critical element in dc parametric testing. Reedholm has developed well guarded, low-noise, low-thermal crosspoint switch modules using dry-reed relays. Long relay lifetimes are assured by eliminating hot switching. That is why Reedholm prevents hot switching at the lowest driver level. However, it is virtually impossible to offer a dc parametric test system immune to the effects of hot switching under all possible situations. But if the electrical interactions between test equipment, test structures, and parasitic devices, are understood, hot switching can be virtually eliminated.

Hot switching damage occurs when a relay contact conducts enough current to cause an arc when opening. Such arcs transfer materials from one contact to another. If long enough, an arc can weld contacts. Even if welding does not occur, material transfer leads to contact degradation that can continue even if there is no additional arcing.

Not much voltage is needed to create an arc. Actual voltage is a material property of the metal surfaces involved, and is around 7V for dry reed switches. But keeping switched voltages below the arc voltage is not enough. When a current path is opened, back emf from wiring inductance or instrumentation can easily create a voltage much higher than the arc voltage threshold.

Instrumentation reed relay vendors specify purely resistive loads in lifetime guarantees of $>10^8$ operations. Switching voltages are generally <5V with capacitive loads <50pF. However, some are able to specify up to 12V switching.

Parasitic Hot Switching

Software can eliminate hot switching from known causes. Delays, status checking, measurements, rules for switching are added or modified as Reedholm identifies and removes potential hot switching. However, software solutions are not possible if the source of hot switching is not known or under control.

Parasitic hot switching happens when a test structure charges capacitance that cannot be discharged under software control. Figure 1 is a schematic of a BV_{ces} test that would induce hot switching through parasitic diode CR_p to the wafer backside. Pins 1, 2, and 3 provide connection and control of the transistor. Pin 4 represents an unused matrix pin and its attendant cable capacitance, C_c. Capacitance C_p represents that of a chuck in ohmic contact with the wafer backside. Relay contact K_g represents the pin 4 relay that will connect pin 4 to ground at some time, thereby discharging the parallel combination of C_p and C_c.

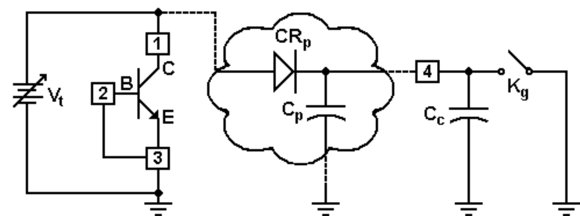

Figure 1 – Chuck and Cable Charging

Parasitic Capacitance Values

The capacitors are much larger than the 50pF maximum specified by reed relay vendors. Depending upon chuck type and size, C_p can range from a few hundred to several thousand picofarads. Unless identified as low capacitance, hot chuck capacitance can be quite large and approach 10nF.

Cable capacitance is seldom a concern in parametric testing because active guarding reduces the capacitance between shield and signal path to virtually zero. However, when a pin is not connected to a supply or meter with active guarding the 30 to 50pF/foot capacitance becomes several hundred picofarads for a few feet of cabling.

Test Time Relationships

Figure 2 illustrates what happens in a BV_{ces} test in which substrate/chuck charging occurs. Waveforms V_t and V_d are the voltages on pins 1 and 4 respectively.

At time t_0, power supply V_t, ramps voltage on pin 1 to V_T. Voltage on test pin 4 follows V_t minus the forward voltage drop across CR_p. At time t_1, power supply V_t ramps down to 0V, thus returning the voltage at pin 3 to 0V. However, during ramp down of V_t, CR_p reverse biases, leaving the wafer chuck and cable capacitance of pin 4 charged to V_D.

The latest Reedholm power down software grounds all pins once the test system has been returned to a safe condition based on the applied biasing. That time is represented as t_3. Since voltage is not expected on an unused pin, closing K_g discharges the paralleled capacitor with little to no current limiting. That hot switching event can easily weld a relay contact.

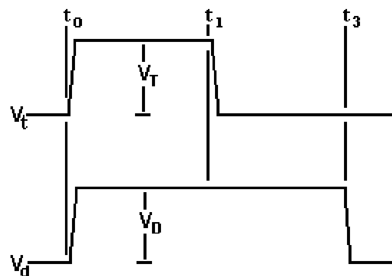

Figure 2 – Voltages at Pins 1 and 4

Emulation Waveforms

Figure 3 is a crude emulation of the hot switching scenario of Figure 1. Capacitance C_p due to the prober chuck is not included since it is effectively always in parallel with C_c, so there is no need to consider a separate capacitor. Measurements of the combination of Tester Analog Cable (TAC), Prober Analog Cable (PAC), and low leakage 24-pin probe card showed pin to shield capacitance to be 534pF.

Power supply PS1 was used to force 5mA, with 100V compliance, into pin 8. Resistor, R_{ts}, represents a test structure connected between pins 8 and 9. Having a transistor as the structure would have made this example more complex without adding to illustrating the events. A small signal, low leakage diode CR_P emulates a parasitic path to pin 16, which is disconnected from the test.

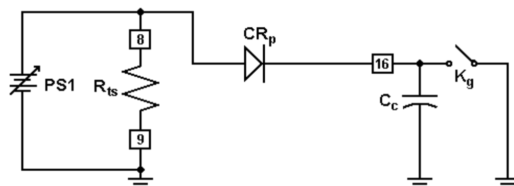

Figure 3 – Emulation of Parasitic Structure

Channel 1 of the oscilloscope screen capture of Figure 4 shows the voltage waveform due to PS1 driving test pin 8. There is some overshoot as PS1 comes out of current limit at t_a. On the trailing edge, voltage ramps to 0 starting at t_b. There is some apparent recovery as the power down routine puts PS1 and other resources into the desired state. Channel 2 monitors the voltage at pin 16, the emulated charging path. Voltage overshoot is a little higher on channel 2 at t_a because the emulation diode prevents current flow required for quick recovery as voltage mode is established.

Voltage droop on channel 2 from t_b to t_c is due to the 10MΩ scope probe discharging C_c. Despite the discharge, almost 30V remains on the capacitor at t_c, and all of that charge is discharged to ground through relay K_g at the end of the test cycle.

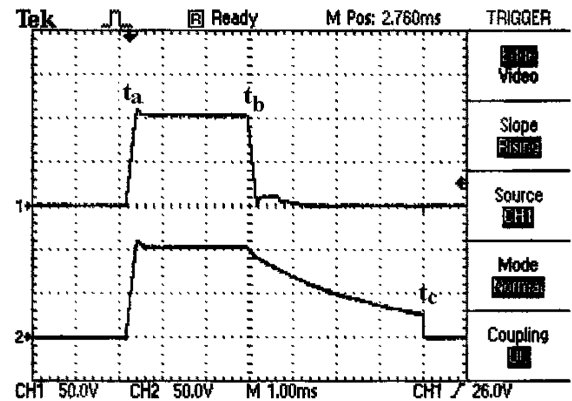

Figure 4 – Cable Capacitance Only

Figure 5 shows how increasing capacitance by 500pF to represent a chuck increased stored charge at the end of the test cycle time to 65V from 30V.

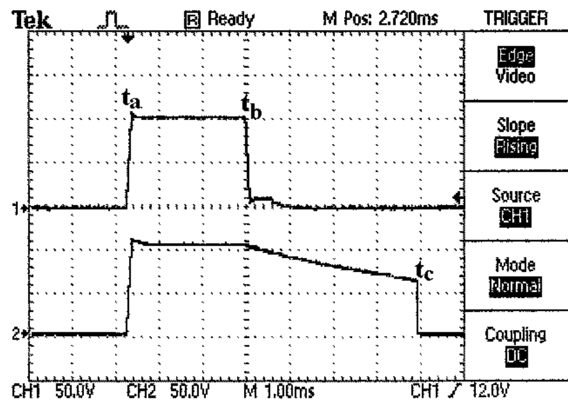

Figure 5 – Cable Capacitance + 500pF

Preventing Parasitic Hot Switching

Hot switching is best avoided by starting with test structures that do not have extra connections to test pads. With wafer real estate continually at a premium, that is not always possible, but it is possible to be sure that all connections are documented. This includes:

- Pad to pad interactions
- Chuck biasing/loading
- Effects of probe cards and other fixturing

Once the electrical layout and interconnections characteristics are understood, test conditions may be created to avoid hot switching if not eliminate it. Unfortunately, sometimes the only thing that can be done is to forgo a test or re-layout the test structure. Fortunately, the ground unused pins option is a quick way to identify suspected hot switching tests.

Isolating Parasitic Hot Switching

Tying pin 16 to ground for the emulation would prevent hot switching and damage to pin 16, but that would obviously prevent getting meaningful data for the test. However, such a strategy can be used to isolate possible parasitic hot switching. That is, grounding unused test pins would be a quick way to identify those tests that could be causing hot switching damage.

Biasing Unused Pins

For the emulation example, the unused tester pins could be driven to the same voltage as the breakdown voltage. One way would be to tie them to a separate supply programmed to the same voltage. However, that solution would require understanding startup behavior of each supply in order that forward conduction or reverse breakdown of the parasitic diode not occur during biasing or voltage stepping.

The best way to avoid effects of the parasitic diode in this example would be to tie the unused pin to the test high pin, i.e., test voltage. That shorts out the parasitic diode and does not let it affect results.

Whether tied to the high pin or biased separately, a supply guard circuit drives cable capacitance so the only extra delay would be that needed to drive unguarded chuck capacitance.

Figure 6 shows what happened when the emulation was used with the unused tester pin tied to the high pin. Notice that the voltage at pin 16 was at 0V well before t_c, thereby avoiding hot switching relay K_g.

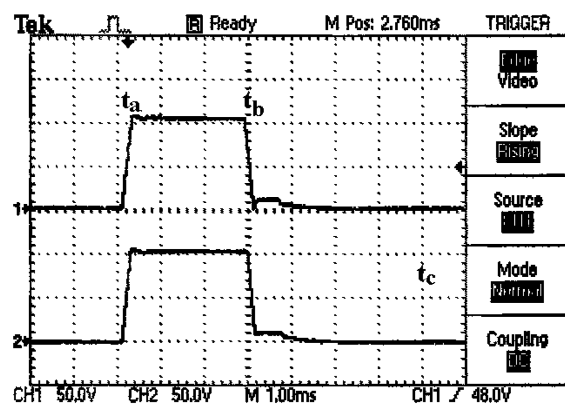

Figure 6 – Tying Unused Pin High

Acquire, Build, ChargeScope, EMAGE, EMPAC, EMREL, Examine, GrafPAC, RDS DOS, and RDS Intranet are trademarks of Reedholm Systems Co. All other company and/or product names are trademarks of their respective companies. Copyright © 2017 Reedholm Systems Co.