TECHNICAL NOTE

TN-106

Electrical Testing of Oxide Quality

Introduction

DC current or voltage forcing tests are used to judge relative qualities of semiconductor insulators from the thinnest tunneling oxides to inter-metal dielectrics two orders of magnitude thicker.

Thicker oxides and inter-layer dielectrics are normally tested to physical failure or breakdown using voltage ramps. The figure of merit is the voltage at physical breakdown indicated by detectable current flow through the device not attributable to displacement current. Sometimes elapsed time is used as the dependent variable, and the figure of merit is time dependent dielectric breakdown (TDDB). Gathering additional information, such as charge to breakdown (Q_{BD}), is difficult since electron avalanche normally occurs earlier in the ramp than onset of measurable tunneling current [1].

Thinner oxides are also evaluated using voltage breakdown, but since they do support tunneling currents, it is possible to generate data sets of current, voltage, and time triplets from which Q_{BD} can be determined.

While voltage breakdown testing permits little discrimination within a population [4], testing for Q_{BD} does. However, making good Q_{BD} measurements is much more difficult. It requires sound characterization of current, voltage, and time measurement uncertainties. The same care that permits good Q_{BD} measurements also permits extraction of additional parameters like bulk and interface trap densities [7], oxide thickness [8], etc.

Test Requirements

This note is concerned with gate oxide electrical testing issues and concentrates primarily on test requirements for gathering high quality data. While this note does not delve into test structure design, gathering oxide data has little value if test structures are poorly conceived or implemented. They are a critical ingredient in the creation of quality data.

Importance of Test Structure Design

Test structures are like any other tools; i.e., their purpose and scope should be defined prior to their design. Whether in development or production, their use should lead to information which can be acted upon. Incorporating diagnostic capabilities requires a broad knowledge of both processing and testing which takes several years to acquire. Delegating test-structure design to untrained and inexperienced engineers is a formula for poor quality data.

Reliability and Parametric Data

Effective wafer level reliability testing demands the highest quality data. Levels of data ambiguity which could be ignored in parametric data might hide the tail of a sub-population exhibiting early wearout. Thus, if 1,000 reliability structures were tested on a wafer lot, even one ambiguous result would be quite costly because:

- If it were a false indicator, considerable additional test time and failure analysis would have to be undertaken, and thus wasted, in case it indicated a true reliability problem.
- If a problem were missed indicating a defective sub-population, there is no other method of finding it. Unlike parametric testing which can be validated by yield results, there is no practical method of quickly finding defective sub-populations if missed at wafer level testing. Such problems are only found by customers or during high volume, extended burn-in tests.

Fowler-Nordheim Relationship

Once suitable structures are available, gathering good test data requires an understanding of how device characteristics affect instrumentation performance. Fortunately, gate oxide behavior has been well characterized. There is general agreement that the Fowler-Nordheim (FN) equation for field emission from a conducting surface describes oxide behavior quite well over a wide range of oxide thicknesses. Oxides thinner than 5nm are subject to direct tunneling and require a different conduction model [10] that isn't covered in this note. However, the low current sensitivity requirements would be the same for direct tunneling measurements.

A few equations are derived below for estimation of current sensitivity test requirements. For the FN equation below, current density (J) in amps/cm^2 is related to the electric field (E) in MV/cm and the constants A in amps/MV^{2}and B in MV/cm.

$$J = AE^2 e^{-B/E} \quad (1)$$

While use of electric field and current densities is appropriate when describing physical behavior, from a test viewpoint only the voltage and current levels are important. By introducing current (I) and area (a), Equation (1) can be re-written as:

$$I = aJ = aAE^2 e^{-B/E} \quad (2)$$

Although the FN equation seems to hold over a wide range of currents, there are practical limitations to finding the current associated with each voltage. In fact, the predicted tunneling current at low fields is beyond the low current capabilities of any measurement instrumentation.

Converting Equation (2) by taking its logarithm:

$$\log(I) = \log(aA) + 2\log(E) - \left(\frac{B}{E}\right)\log(e) \quad (3)$$

In this note, values for constants A (1.25×10^6A/MV^2) and B (233.5MV/cm) were taken from the Nissan-Cohen et al. [11] paper which assumed field emission from the silicon surface.

For a structure area of 10,000μm^2, the current versus field relationship, with I in amperes and E in MV/cm, becomes:

$$\log(I) = 2.194 + 2\log(E) - \left(\frac{101.4}{E}\right) \quad (4)$$

The shape of the FN graph of log (I) is dominated by the last term in Equation (4), so except for an area dependent offset, the log of the tunneling current increases with applied field. The second term is not much of a factor for fields below 5MV/cm, but its effect increases the value of I by two decades when the field reaches 10MV/cm.

Measurement Sensitivity Requirements

In practical terms, a 5 volt bias on a 10nm thick oxide with an area of 10,000μm^2 produces a 5MV/cm field and a predicted tunneling current of around 0.2fA. The capacitor area would have to be five orders of magnitude larger, or 10cm^2, to produce a predicted current in the picoampere region.

For volume testing of oxides using an automatic prober, it is practical to make measurements down to the 100fA level, but even that level would require a 1cm x 1cm structure for detection if no thinning defects were present.

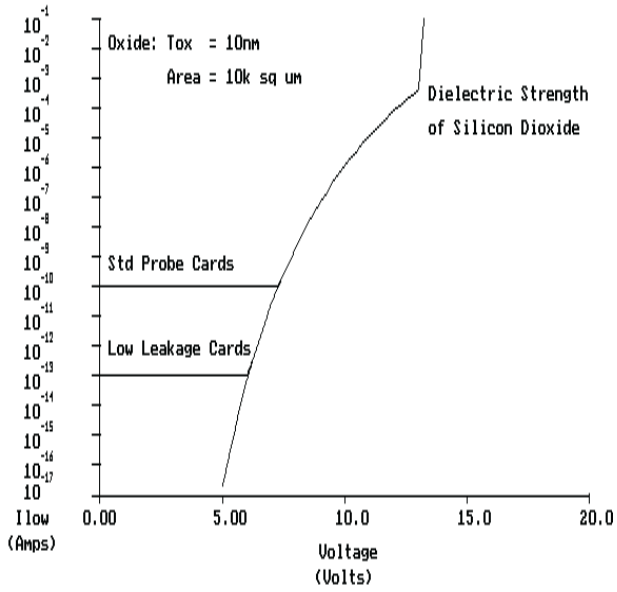

Figure 1 - Idealized FN I-V Graph

Impact of Defects on Tunneling Current

The preceding comments illustrate that tunneling current measurements are only practical at relatively high fields. Thus, an oxide that insulates near zero volts yet conducts current at voltages well below intrinsic breakdown must have defects which produce localized high fields. Presence of unexpected tunneling can provide information about the nature of defects. These may be present in combination so structures need to be designed to isolate effects.

- Small area thinning produces excess current at very low fields before changing slope or "walking out" to meet the intrinsic graph [5].
- Bulk trapping causes larger slopes at high current densities [12].
- Either large area thinning or process charging can cause lateral translation of the graph [12,14].
- Interface traps or series resistance cause the graph to decrease in slope near breakdown [9].

Figure 1 is an idealized FN field-current graph of a 10,000μm^2 oxide structure. Note the limits that probe cards place on current sensitivity in practical automatic systems.

Thickness and Area Extraction

If an oxide structure is sufficiently defect free, its thickness or area can be extracted from any point on the FN voltage-current graph when tunneling current is present [13]. Sophisticated, multi-point techniques are used to minimize uncertainties. High trap levels, oxide charge, or series resistance have to be detected and either eliminated or accommodated for extraction to be effective [16].

Device Resistance Considerations

As just described, limitations of dc instrumentation used for oxide wearout testing restrict FN data gathering to relatively high fields. However, even if fields are high enough to produce adequate tunneling current, there are additional instrumentation requirements which must be addressed if high quality FN data is to be taken.

One of the major impacts on instrumentation performance is the device under test source impedance. If it is very high when measuring voltage, care must be taken that the input impedance of the voltage measuring instrument does not cause a significant reduction in the voltage being measured. Conversely, if it is too low when measuring current, measurement uncertainties can be multiplied and measurement times increased.

The effect on tunneling current of small changes in field strength is found through differentiation of the FN equation.

$$\frac{dI}{dE} = aAe^{-B/E}(2E) + aAE^2\left(\frac{B}{E^2}\right)e^{-B/E} \qquad (5)$$

Extracting the expression for I from each term:

$$\frac{dI}{dE} = I\left(\frac{2}{E} + \frac{B}{E^2}\right) \qquad (6)$$

Since the second term is so much larger than the first, the equation is rearranged:

$$\frac{dI}{dE} = \left(\frac{BI}{E^2}\right)\left(1 + \frac{2E}{B}\right) \qquad (7)$$

For much of the range, $2E/B$ is < 1 so it can be ignored. Even at a field strength of 10MV/cm, the term's contribution is only 5% of the ideal oxide's small signal resistance. Thus, the approximation for dI/dE is:

$$\frac{dI}{dE} = \frac{BI}{E^2} \qquad (8)$$

Inverting the differential relationship and using $E = V/t$ where V is the test voltage and t is the oxide thickness, Equation (8) becomes:

$$\frac{d(V/t)}{dI} = \frac{(V/t)^2}{BI} \qquad (9)$$

Multiplying both sides by t:

$$\frac{dV}{dI} = \frac{V^2}{BIt} \qquad (10)$$

The equation can be rearranged, using $E = V/t$, to provide:

$$\frac{dV}{dI} = \left(\frac{V}{I}\right)\Big/\left(\frac{B}{E}\right) \qquad (11)$$

Equation (11) provides simple insight into what the small signal resistance might be. As the slope of the FN I-V graph is quite steep over much of its range, the term B/E is relatively constant over a wide range. Thus, the small signal resistance is simply the ratio of its voltage and current divided by a number varying from 46 at 5MV/cm to 23 at 10MV/cm based on a value of 233.5MV/cm for B.

For the data plotted in Figure 1, a current of approximately 1μA would flow at a voltage of 10V, so the small signal resistance would be (10V/1μA)/23 or approximately 440kohms. At that level, the input resistance of the voltage measuring instrument (when forcing current)

would have to be more than 40Mohms to keep dynamic voltage errors below 1%.

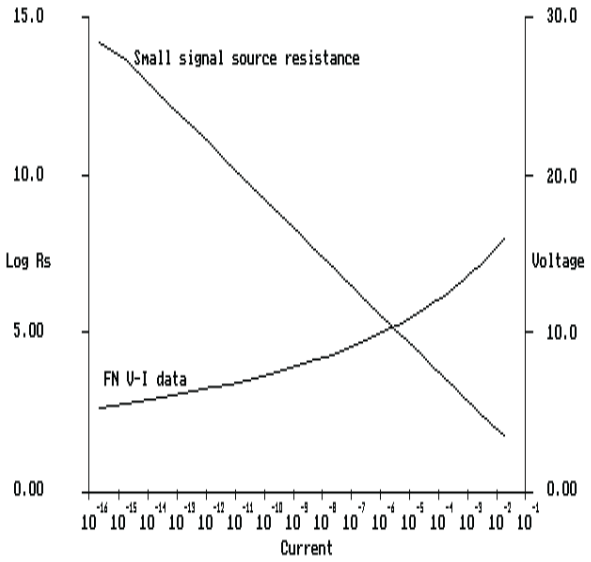

Figure 2 - Idealized Small Signal Resistance Graph

Put into perspective, conventional system digital multi-meters have input resistances of 10Mohm at breakdown voltages above 10V. Of course, a 40Mohm resistance would conduct 250nA at 10V, or 25% of a tunneling current of 1μA. Thus, the dc input resistance would have to be more than 1Gohm to have less than 1% effect on a tunneling current of 1μA.

Figure 2 illustrates small signal resistance as well as field voltage for the graph of Figure 1. Figure 3 illustrates the loading effects of a meter with finite input resistance.

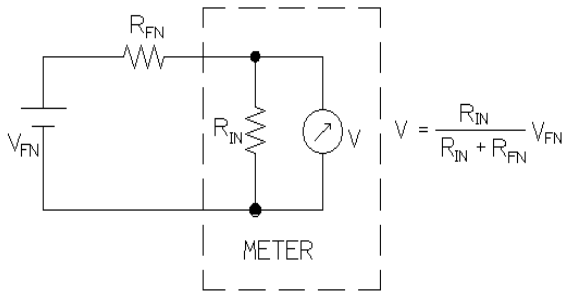

Figure 3 - Finite Input Resistance

Types of Wearout Tests

From an electrical testing viewpoint, oxide wearout tests are simply voltage versus current tests with elapsed time as a third variable. They are true reliability tests in that oxide structures are measured prior to stressing and then stressed to failure over a known time period. Thus stress can be determined and a test sample ranked according to lifetime.

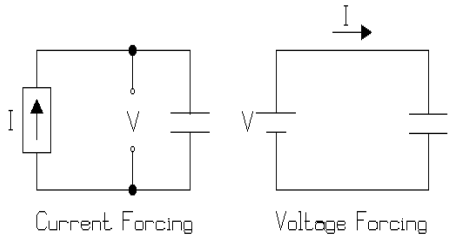

Figure 4 - Test Circuit Configurations

Either current or voltage is used as the independent forcing function shown in the simplified test configurations of Figure 4. Test types can be grouped into three categories:

- Constant Stress Current or Voltage
- Ramped Stress Current or Voltage
- Ramped and/or Constant Current or Voltage

Constant Voltage Stressing

Constant voltage oxide testing is usually restricted to long term stressing of packaged test structures to produce TDDB data. For such applications, field strengths are closer to use conditions than breakdown, and tunneling currents are extremely low. It is often impractical to measure Q_{BD} with constant voltage since the only current being measured is the instrumentation noise level. However, constant voltage stressing of packaged structures may be the only way to gather data that correlates to real world failures [15]. Also, the lack of clear agreement on failure mechanisms sometimes forces stressing at such low fields that tunneling currents, and thus Q_{BD}, cannot be measured.

On the other hand, constant voltage stressing can be used to induce high levels of tunneling when structures are uniform and exhibit essentially intrinsic behavior. Thus, some fundamental investigations using constant voltage permit measurement of Q_{BD} with high confidence [10].

Voltage Ramp Stressing

Typically, voltage ramps are used to generate the FN *I-V* graphs shown in Figure 1. A JEDEC committee has documented a standard voltage ramp, or Vramp, with which several test system suppliers comply. Voltage ramp stressing adds the feature of increasing oxide voltage linearly with time. Since elapsed time is proportional to voltage, Q_{BD} is effectively the area under the FN *I-V* graph.

Voltage ramp failure data correlates well with TDDB data from constant voltage stressing, and ramp testing can be quite fast without losing correlation [17]. In practice, testing is so quick that devices can be stressed sequentially on an automatic prober instead of using parallel techniques.

Combination Voltage Stressing

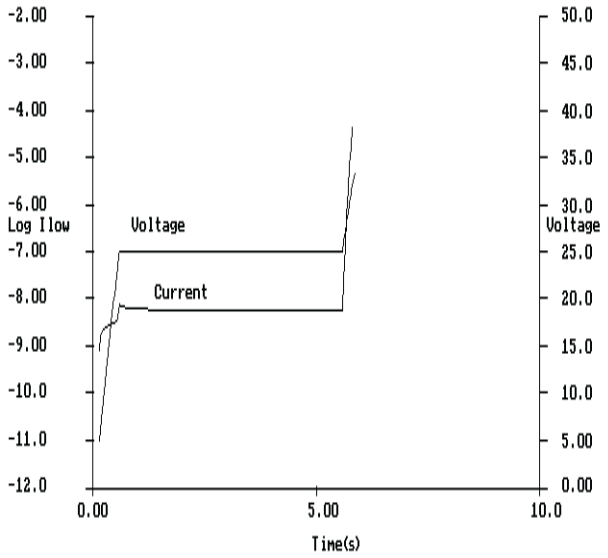

Figure 5 - Voltage Ramp with Constant Stress

Combining voltage ramping with a constant voltage period provides additional information about oxide quality:

- If constant voltage Q_{BD} is desired, ramping up to the stress level permits discrimination among failures which occur at lower voltages. Thus, if Q_{BD} at 7MV/cm is monitored, ramping to 7MV/cm from 0V would provide a distribution of breakdowns below 7MV/cm which could be used in problem diagnosis.
- If ramped Q_{BD} is measured, a decrease in tunneling current at constant voltage indicates local field reduction through electron trapping. The level of charge trapping is a function of current change over time.
- A period of constant stress can be used to provide a dramatic separation in time of early failures from the normal population. For instance, the five seconds of constant stress shown in Figure 5 could be used to separate the failures happening below 25V from those which happen at higher voltages.

Constant Current Stressing

One of the simplest methods of measuring Q_{BD} is to force a constant current until breakdown is indicated by a sudden reduction in the oxide voltage [13]. By forcing tunneling, the entire structure is potentially stressed at the intrinsic FN voltage. However, defects can dramatically affect the FN voltage resulting from a given current.

Defects which imply significant thinning may have enough current funneled through them to create electron traps which, on being filled, act to reduce the local electric field producing electron emission. Reduction of the local field lowers the defect tunneling current and the overall tunneling current is seemingly unaffected.

If defect areas are large enough, they hold the FN voltage to a lower than intrinsic level until the traps are filled. Then the voltage "walks out" to the intrinsic FN voltage. Such structures exhibit Q_{BD} data indistinguishable from those of defect free ones.

On the other hand, defect areas that are too small never establish electron traps or fill them, so current funneling is not reduced, and even low current densities can be enough to cause very quick failures.

A significant problem with constant current stressing is that defect-free capacitors take a great deal of charge compared to the normal population. Since the time under test is proportional to charge passed through the oxide, the span of test times is as large as the span of Q_{BD}, and that can be at least six orders of magnitude. Thus, if a minimum acceptable test time were 10ms, the maximum time could be 16 minutes.

Current Ramp Stressing

The large variability in time required for constant current Q_{BD} measurements is what makes current ramp stressing so attractive. With this method, current is increased logarithmically versus time and the resultant voltage measured for each increase in current. As a companion to the Vramp test, the JEDEC committee on oxide testing documented a standard current ramp, or Jramp, with which several test system suppliers comply.

The test problem of maintaining adequate sensitivity to defects without placing severe requirements on test systems is addressed with the current ramp [6]. While mainly used for thin oxides, some papers have reported successful use of current ramp testing on oxides up to 110nm thick [2].

Combination Current Stressing

As with voltage stressing, combining current ramping with constant current stressing as shown in Figure 6 provides additional information about oxide quality:

- If constant current Q_{BD} (sometimes termed fluence testing) is desired, ramping up to the stress level permits discrimination at a particular quality level. Thus, structures which might register as being initially shorted could be segregated according to defect size by ramping from a much lower current level.
- If ramped Q_{BD} is more important, an increase in voltage during the constant period usually indicates electron trapping within the oxide while a decrease usually indicates creation of interface traps. The amount of trapping can be quantified from the voltage changes.
- Instead of using slow ramps [3], a period of constant stress can provide dramatic separation in time of early failures from the normal population. Thus, the constant stress could be set at a level that segregates structures with small area defects from those which will trap out and behave essentially like intrinsic structures.

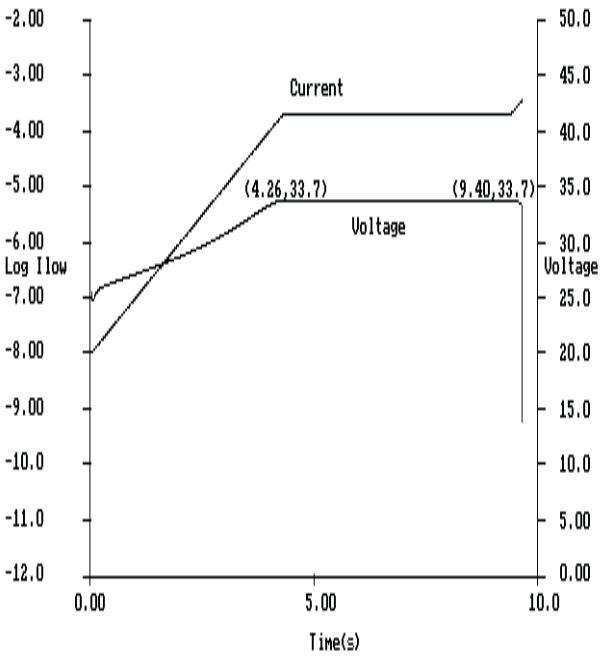

Figure 6 - Current Ramp with Constant Stress

System Specifications & Accuracy

Since Q_{BD} measurements are essentially an integration or summation of current-time product (Q_{BD} = current * elapsed time), uncertainty in Q_{BD} data is as dependent on timing data as it is on current.

For voltage ramping techniques, measurement time intervals have to be very short in order to measure the charge which flows rapidly with onset of breakdown. If they aren't, the ability to compare data with that from other forcing methods is severely compromised. For current ramping, the ability to make high quality Q_{BD} measurements is limited by instrumentation speed.

Timing uncertainty is highest for short time periods, and is reduced over the total time for many periods. If the uncertainty per period is normally distributed, then the uncertainty in total time will also be normally distributed with a value equal to the root-mean-square sum of all periods. Equation (12) shows the relationship between intended total elapsed time (T), number of timing intervals (P), intended discrete time interval (τ), and the uncertainty within each interval (ξ).

$$T = P\tau\ (1 \pm \xi / \sqrt{P}) \qquad (12)$$

Timing Accuracy & Operating Systems

The test computer operating system (OS) can have a dramatic effect on timing accuracy. A single tasking OS like MS-DOS can be used to provide strict control linked to computer's crystal clock with uncertainties measured in parts per million. As a single tasking OS does not share tasks, there is never any ambiguity in event timing or instrument control. With a Pentium III processor operating at 800MHz, times can be measured and predicted with uncertainties less than 10ns.

With a multi-tasking OS, lack of full control must be overcome if timing data are to be accurate. However, that is not simple. As absolute control is never passed to an application program in a multi-tasking OS, time keeping is done by a real time clock.

Since events such as time-to-breakdown are unpredictable, there is always a significant probability that the OS kernel will be servicing another task even when a single application is running. Thus, the computation of timing uncertainty must include the maximum time it takes to service competing tasks and the latency of accessing the real time clock. That is why timing uncertainties with multi-tasking

operating systems are much worse than those under MS-DOS.

If elapsed time is poorly known or controlled, a constant stressing condition is often the only sure way of correlating data among different sets of test equipment.

Instrumentation Requirements

The basic source and measurement instrumentation required for oxide wearout testing is available from multiple vendors. If sufficient judgment is used in their selection, discrete instruments are available from which adequate systems can be built. In addition, there are commercial automatic systems which eliminate the need for system design and documentation.

Automatic systems are virtually a necessity because a lot of data are needed to characterize defects. Gathering statistically significant sample sets manually is very time consuming. While it is possible to build automatic systems from discrete instruments, suppliers of commercial systems address several needs that are seldom addressed with in-house systems:

- Specifications including effects of all components
- Cabling error source elimination
- Subtle software error elimination
- Self test software, fixtures, and documentation

Whether a full system or discrete instruments are used, it is important to consider the impact of guaranteed instrumentation specifications on measurement performance.

Instrumentation Specifications

Over most of the intrinsic tunneling regime, adequate current and voltage sensitivity is available with modern dc parametric test systems. As noted previously, certain system instrumentation may not have the desired characteristics.

Parametric test systems have measurement uncertainties < 0.1%, use remote (or Kelvin) sensing which can assure delivery of voltages with that same level of precision, and have current source accuracies which are not compromised by small signal resistance of tunneling oxides. Thus, for oxide testing, voltage instrumentation in dc parametric test systems address three important requirements:

- Small measurement uncertainty compared to the distribution of voltages across a sample set. As breakdown voltage distributions can be ±50%, a 0.1% voltage measurement uncertainty is insignificant.
- Small effect on tunneling current. As peak-to-peak current noise in practical environments is several hundred picoamperes, current forcing experiments must induce currents several times higher. Thus, offset current of the voltmeter can be quite large, or much worse, than commercially available system voltmeters.
- Kelvin, or remote, sensing of delivered voltage so that current flow to large area capacitors is not reduced by resistance in series with the voltage source. This technique uses four connections, two souring and two sensing, to the device under test so that any voltage drop along the sourcing leads is not between the sensing leads in the measurement circuit. Thus, the voltage sensed is due entirely to the device's reaction to the current being sourced.

While voltage measurement and forcing present few problems, most users of dc parametric test systems have had difficulties with low level current measurements. As a result, there is a pervasive, but mistaken, belief that automatic sub-picoampere measurements are an art form with unpredictable results. That isn't true! It is practical to make dc current measurements down to, and below, 1pA on an automatic prober under high speed operation.

Resolution and Error Specifications

Digitizing resolution is often the only specification used to compare systems intended for very low current applications. However, resolution is seldom an important factor in specifying possible errors in a measurement system. Analog gain, linearity, noise, and offset are much more important.

Possible analog errors are investigated thoroughly by instrumentation designers in establishing the foundation for published specifications. Such specifications for analog errors cannot be ignored because predicted errors are so much larger than the digital resolution. The predicted errors can, and do, occur. Furthermore, instrumentation is guaranteed only to the error specifications, not to the digital resolution displayed on the front panel or the CRT screen.

Current Error Sources in DC Test Systems

A dc parametric test system is only as good as the weakest element in the path from instrumentation to device. Unless all contributors to measurement errors are properly addressed, the excellence of a particular element will usually be obscured.

Thus, the 1fA sensitivity of a current meter is unattainable through a matrix with self-generated error currents of 1pA. Conversely, a probe card with leakage of 0.01pA/V is overkill if the current meter offset is 15pA.

An automatic system capable of fast, low current measurements has numerous sources of possible errors. Those sources can usually be associated with one of three sub-systems, or elements:

- Instrumentation
- Matrix
- Probe Card plus Fixturing

A system matrixdiagram of a dc parametric test system is shown in Figure 7 with the low current matrix required for ultra-low oxide measurements.

Error or Uncertainty Calculations

By convention, instrumentation companies represent the possible uncertainty distribution at any particular condition as a linear function of the parameter value under consideration. The coefficient of the parameter value is usually termed "gain error," and the constant term is usually termed "offset error." (From the viewpoint of most users, the term, "uncertainty" is probably more meaningful than the hard and fast term, "error.")

Error = (Gain Error * Value) + Offset Error

Most specifications have more than two terms and more than one dependent variable. That is especially true of instrumentation approaches in which both output current and output voltage affect current accuracy. However, all terms can be reduced to a simple linear equation when a single output test condition is used to compare accuracies.

Example Error Calculation At 10pA

Specifications published by three vendors of dc parametric test systems were used to calculate the error limits shown in Table 1. The instrument column contains the errors attributable to the system instrumentation, the matrix column has those errors where published, and the fixture column contains errors attributable to the probe card plus any fixturing into which the card may be inserted.

Current Measurement Errors Including Probe Card			
	Instrument	**Matrix**	**Fixture**
Vendor A	1.0% of Value + 8pA	N/A	0.1pA/V
Vendor K	0.5% of Value + 15pA	1pA + 0.1pA/V	0.1pA/V
Vendor R	0.2% of Value + 250fA	Included	0.01pA/V

Table 1 - Published Error Terms, Iout = 10pA, Vout = 0

For each system, the most favorable ranges were picked to minimize the error which could accrue from measuring a 10pA sub-threshold source current with 100mV of drain bias, 5V of gate bias, 0V of substrate bias, and 0V of source bias.

Current Leakage Errors

The ratio terms (e.g., 0.1pA/V) in Table 1 indicate the additional effect of biasing voltages on either side of a matrix pin being evaluated. The worst case condition typically occurs when the bias is placed on an adjacent pin. Current leakages shown in Table 2 were computed with a V_{GS} bias of 5V, V_{DS} of 100mV and includes contribution from the probe card. Possible leakage currents were added to the instrumentation errors to provide total offset errors. Gain errors were computed for a current measurement of 10pA. The total possible error, or uncertainty, was computed by adding the offset and gain errors.

Leakage Current Offsets (Instrumentation Only)	
Vendor A	5.1V * 0.1pA/V = 0.51pA
Vendor K	5.1V * (0.1 + 0.1)pA/V = 1.02pA
Vendor R	5.1V * 0.01pA/V = 0.05pA
Offset Errors (Leakage Current + Instrumentation)	
Vendor A	0.51pA + 8pA = 8.51pA
Vendor K	1.02pA + 15pA = 16.02pA
Vendor R	0.25pA + 0.05pA = 0.30pA
Gain Errors	
Vendor A	1.0% of 10pA = 0.10pA
Vendor K	0.5% of 10pA = 0.05pA
Vendor R	0.2% of 10pA = 0.02pA
Total Error at 10pA	
Vendor A	8.61pA or 86.1%
Vendor K	16.07pA or 160.7%
Vendor R	0.32pA or 3.2%

Table 2 - Cumulative Error for 10pA Measurement

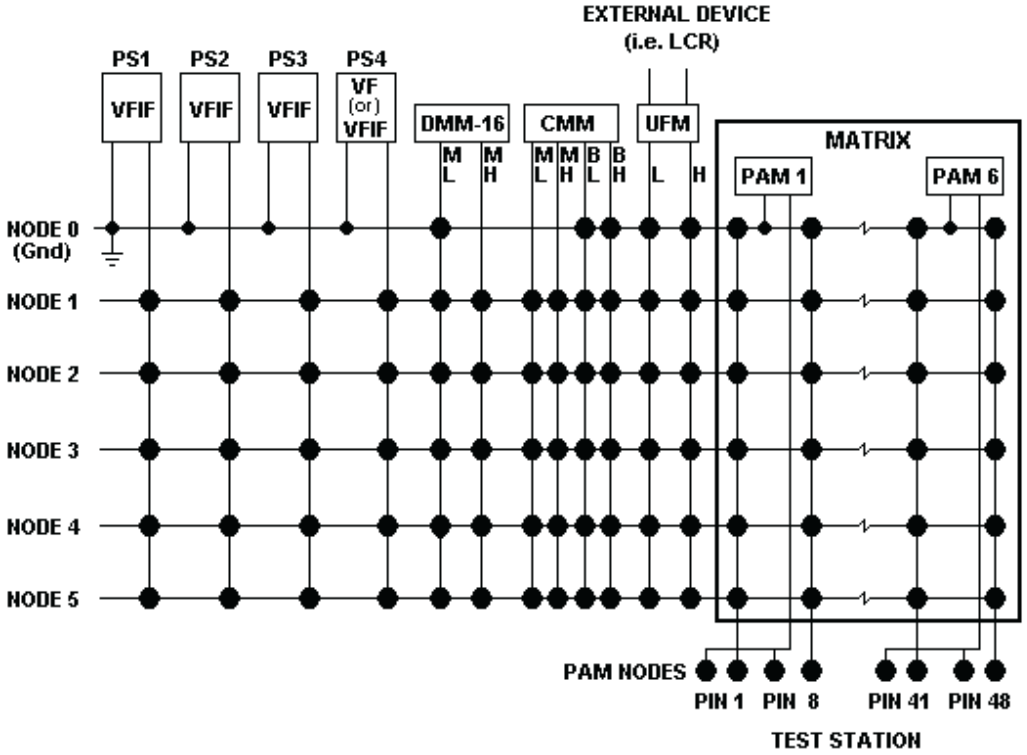

Figure 7 - PAM-Based System Matrix Diagram

Repeatability and Performance

Fortunately for users, most systems perform much better than specifications imply. Certainly, the repeatability of a single system is normally much better than the overall performance specification. However, since specifications are statistically derived, data from any two seemingly identical systems can be quite different even though both are within specified performance limits. That is one of the reasons why correlation between sites, or between development and production, is sometimes an arduous task.

Correlation problems also occur when confidence levels of measurements aren't rigorously determined. Usually, the spread of process parameter uncertainty is much larger than measurement uncertainty. That is, a 10% span in oxide breakdown voltage would indicate fairly good process control, and the normal measurement uncertainty would be a fraction of that at < 0.1%. However, selection of test conditions can change that relationship.

For instance, a hypothetical probability density function (PDF) of breakdown is shown in Figure 8. If a voltage ramp with step size of 5V were used, only the 15V step would produce a result. Thus the distribution of data would have zero sigma and variance. If the test were made more accurate by reducing the step size to a few millivolts, the resultant data would closely match the actual distribution, but would, at first glance, be less "accurate" than using 5V steps. Of course, a cursory investigation would address such a discrepancy. In practice, most static measurement differences among test systems can be resolved with rigorous, but straightforward, computation of uncertainties.

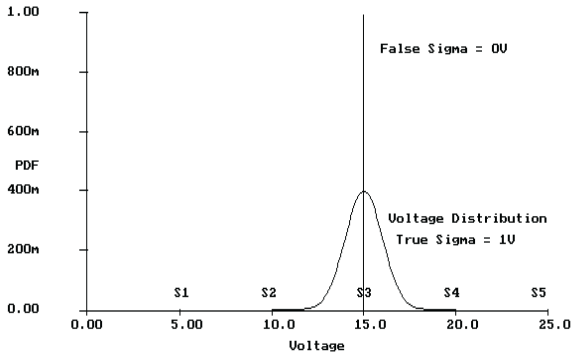

Figure 8 - Hypothetical Breakdown Distribution

Data Quality as a Process

In essence, a test system is part of a process intended to produce quality data. Measurement uncertainty is the measure of data quality and is not difficult to determine. Often the various contributors, or inputs to the data quality process, can be added statistically: i.e.; their contribution can be found from the square root of the sum of their squares; as shown previously, data quality is not related to repeatability.

Unfortunately, dc test systems are often relegated to "black box" status, and attempts are made to "characterize" performance without regard to data quality contributors. In essence, such approaches attempt to control output of a process with several independent inputs. It makes the acquisition of quality data excessively complex and does not work. Only by controlling inputs can data quality be assured.

Nevertheless, this practice occurs whenever a test system model and software are transferred as part of a manufacturing process. If fact, test systems are tools for producing the same results given the same inputs. They should not be considered part of the manufacturing process any more than a wrench is part of an automobile.

Inputs, or contributors, to the data quality process include test conditions, test environment, timing conditions, algorithms, specifications, and physical laws. Sometimes the desired inputs are inconsistent or incompatible. For instance, it might be desired to measure currents beyond the range of any available instrumentation. The rest of this note deals with some important inputs to data quality.

Ideal Current Meter Performance

For semiconductor characterization and monitoring, current measurements are made with a feedback ammeter. Alternate techniques, such as shunt ammeters, are fraught with problems [19], and of little interest since none of the commercial dc parametric analyzers rely on them.

Essentially, the feedback ammeter consists of an operational amplifier and a precision feedback resistor or network. The operational amplifier has high open loop gain, well controlled frequency compensation, plus an input stage with low offset voltage, current, and noise. In Figure 9, an ideal operational amplifier is shown transforming the tunneling current into a voltage which will be digitized.

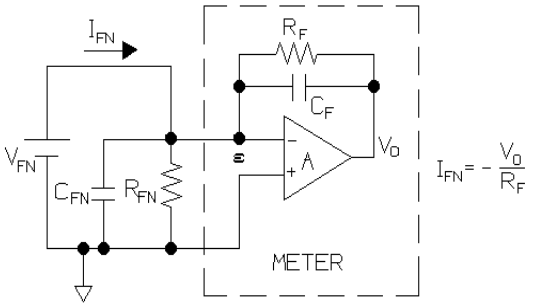

Figure 9- Active Current Meter

Loop Gain Effects

With the exception of impedance loading, voltage measurement circuits are seldom affected by the device under test. That is not true for current measurement circuits. In particular, loop gain is a strong function of the device under test dynamic impedance. Most current measurement instruments are designed to maintain accuracy over a wide range of device impedances, but semiconductor test applications often cause severe problems including:

- Slower than specified time response
- Increased susceptibility to noise
- Reduced accuracy
- Sustained oscillation

For the circuit of Figure 8, the dependence of V_o on I_{FN} can be found through simultaneously solving Equations (13) through (15). Note that Equation (13) is the sum of all currents into the node connected to the noninverting terminal of the operational amplifier. In Equation (13), "s" is the LaPlace operator for the complex frequency term, $j\omega t$, $R = R_F R_{FN}/(R_F+R_{FN})$, $C = C_F + C_{FN}$, and $\omega_a = 2 \quad F_a$.

$$I_{FN} - \varepsilon\left(\frac{1}{R_{FN}} + \frac{1}{R_F} + sC_{FN} + sC_F\right) + V_O\left(\frac{1}{R_F} + sC_F\right) = 0 \qquad (13)$$

$$\varepsilon = -V_o / A \qquad (14)$$

$$A = A_o/(1+s\frac{A_o}{\omega_a}) \qquad (15)$$

Simplified, I_{FN} can be shown to be a second order equation:

$$V_O = -I_{FN} R_F \left(1 + s\left(C_F R_F + \frac{R_F}{R_P}\frac{1}{\omega_a}\right) + s^2 \frac{R_F C_P}{\omega_a}\right)^{-1} \quad (16)$$

Transforming Equation (16) to time domain results in:

$$V_O = -I_{FN} R_F \left(1 - K_1 e^{-1/\tau_1} + K_2 e^{-1/\tau_2}\right) \quad (17)$$

Where $K_1 + K_2 = 1$ and the time constants are determined by finding the roots of the function in Equation (16). For the case of $C_F = C_P = 0$, the response time is determined by the gain bandwidth of the current amplifier. In such a case, Equation (17) becomes:

$$V_O = -I_F R_F \left(1 - e^{-1/\tau_a}\right) \quad (18)$$

Where:

$$\tau_a = \left(\frac{1}{\omega_a}\right)\left(\frac{R_F}{R_P}\right)$$

Note that R_F / R_P is the ratio of the feedback resistance to the summing junction resistance, or the loop gain reduction.

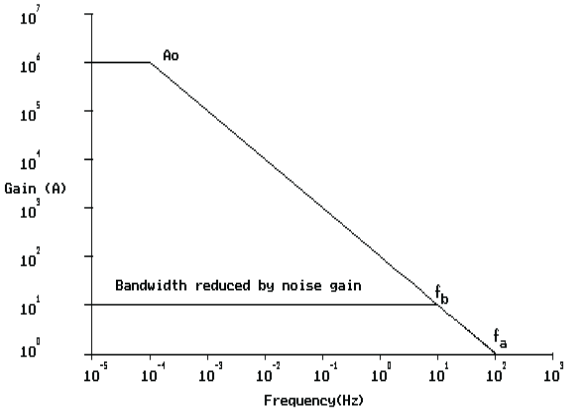

Figure 10 - Loop Gain of Feedback Ammeter

Bandwidth and Time Response

With the introduction of bandwidth considerations for the amplifier as shown in Figure 10, dc performance would not be compromised with a loop gain of 10^5 or 10^6 since those levels of gain would impact accuracy by only 10 and 1 part per million respectively.

However, the introduction of lowered device impedance would affect time response as predicted by Equation (18). (The 100Hz bandwidth is arbitrarily used for illustration and is not meant to represent any particular meter.)

If small signal tunneling resistance is large compared to R_F and C_F is large compared to C_{FN}, there is 100% feedback; loop gain is equal to the operational amplifier's open loop gain. In analyzing dynamic response of the feedback ammeter, the voltage source is replaced by a short circuit; feedback and source impedances are considered as shown in Figure 11. When Z_{FN} is much smaller than Z_F , noise errors are multiplied by the ratio of Z_F to Z_{FN} and loop gain is reduced by a similar amount. The effect on bandwidth of a noise gain of 10 is shown in Figure 10 where bandwidth is reduced from f_a to f_b.

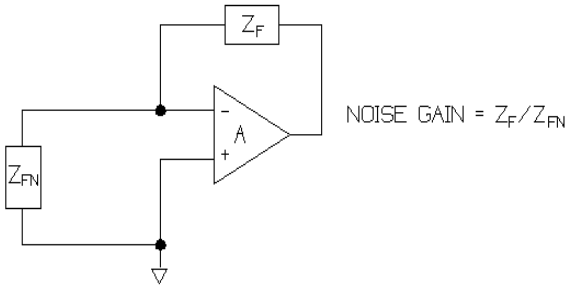

Figure 11 - Noise Gain of Current Meter

As the loop gain characteristic is that of a single pole system, the time response of the feedback ammeter to a step current input at t = 10ms is exponential as shown in Figure 12. Since the bandwidth is reduced by 10 when the noise gain is 10, the step-time response is increased by 10. Such response time degradation is normal in practice. As was noted previously, the small signal tunneling resistance of the ideal oxide depicted in Figure 1 is 440kohms at 1μA. If R_F for the current meter were 5Mohms for 1μA current measurement capability, loop gain degradation would be more than 10, and both the loop gain and response time would be reduced by the same amount.

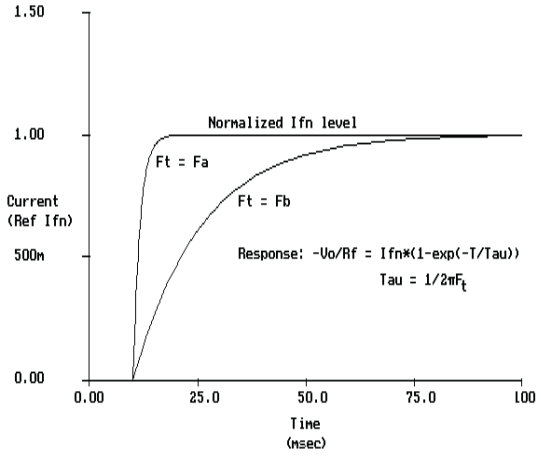

Figure 12 - Time Response to Current Step

The previous equations and comments are provided to show how device impedance can affect test system performance; a special case was used for illustration. More complex computations are normally forgone in favor of computer simulation. Whether done manually or on a computer, errors due to loop gain reduction can be calculated to whatever accuracy is desired. If such calculations aren't made, then dynamic characterization must be done experimentally to insure adequate settling time.

Voltage Overshoot

Independent control of current and voltage settings is a standard feature of sources used in dc parametric test systems. Ideally, when forcing voltage, the current setting limits maximum current to a desired level. Similarly, setting the voltage during current mode operation limits maximum voltage. For each, reaching limit condition causes a transition from one mode to another. There is often little concern about the transition, but oxide testing is not one of them.

For instance, a voltage step might result in a transitory current limit condition while displacement current flows to charge the structure and system capacitance. Thus, the source would transition from voltage mode before the step, to current mode during the step, and then back to voltage mode after the step. There would be a finite delay for each transition with the current to voltage one being critical for oxide testing. During the transition, an over voltage condition would exist. Given the steep slope of the FN I/V curve, even a few volts of overshoot could cause failures in perfectly good oxide structures, and considerable time could be wasted doing analysis on non-existent problems.

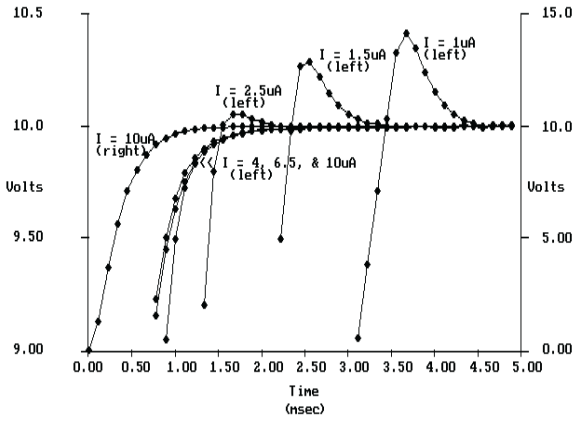

Figure 13 - Voltage Overshoot on 10uA Range

Figure 13 shows the dynamic response of a fast voltage/current source programmed with a 0-10V step and various levels of current limiting induced by displacement current. The axes on both sides of the graph were used, with the right axis having the scale from 0-15V and the left axis having a greatly expanded one. A fast sampling DMM was used to take data in 100µs intervals.

While the maximum overshoot is 0.5V out of 10V and only exists for fractions of a millisecond, it could be that size regardless of the step. As can be seen from the graph, one way to eliminate overshoot is to set the current limit high enough that displacement current does not cause a transition to current mode operation during the step.

Slower instruments have larger overshoot because it is an inverse function of bandwidth. Thus, the only way to eliminate the overshoot while keeping low levels of current limiting is to make the transition occur in zero time.

Cable Capacitance Reduction

There are several errors introduced by practical system analog cabling. Fortunately, the level of cable capacitance is seldom a major problem since the capacitance from signal path to shield is driven to virtually zero by loop gain in the feedback current meter. In Figure 14, the effective input capacitance resulting from the system and instrument capacitance of C_{IN} is reduced by the loop gain factor A.

Dynamically, the reduction ratio varies exponentially with elapsed time. Thus, for a step input current, Z_{IN} would be equal to C_{IN} initially, then decrease to C_{IN}/A_0 after a few time constants determined largely by the bandwidth as reduced by the ratio of C_{IN} to Z_F. While this example is for a grounded current meter configuration, the capacitance reduction occurs when the meter is floating with the shield driven.

When calculating C_{IN}, the entire signal path (internal and external) from current meter to shield termination must be used. Placement of the matrix has little impact on overall capacitance since path length is the determining factor.

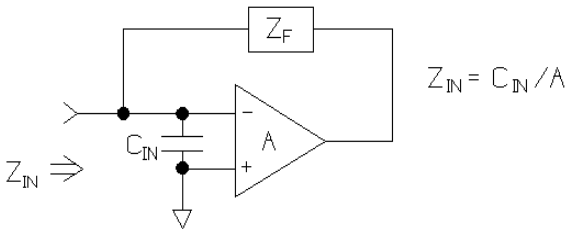

Figure 14 - Reduction of Shielded Capacitance

Shielded cables (co-axial, tri-axial, quad-axial, or twin-axial) have capacitances from 50 to 150pF per linear foot, so six feet of cable at 75pF/foot would present a lumped capacitance of 450pF. Typically, shielded input capacitance of the current meter is a fraction of that value and doesn't materially affect total input capacitance. With a loop gain of 10^7, bandwidth of 1kHz open loop, and a feedback capacitance of 5pF, 450pF would be reduced to 0.045fF with a time constant of around 16ms.

Line Noise Reduction

Although it is possible to come very close to approximating ideal feedback ammeters, noise from the environment often places major limitations on system performance.

Noise sources need to be identified and then eliminated or their effects filtered. Most noise is due to illumination induced conduction changes or line frequency pick-up on non-shielded signal lines. Due to the high impedances seen with oxide testing, ground loops are seldom a problem.

Measurement configuration and structure design can make a significant difference in noise pick-up, but frequently at higher cost than necessary. As Figure 15 illustrates, line synchronous digital averaging can have a dramatic effect on reducing the effects of line frequency pick-up.

Typically, line frequency noise on an automatic prober is less than a few hundred pico-amps without extensive shielding. In creating data for Figure 15, noise was intentionally increased to be discernible.

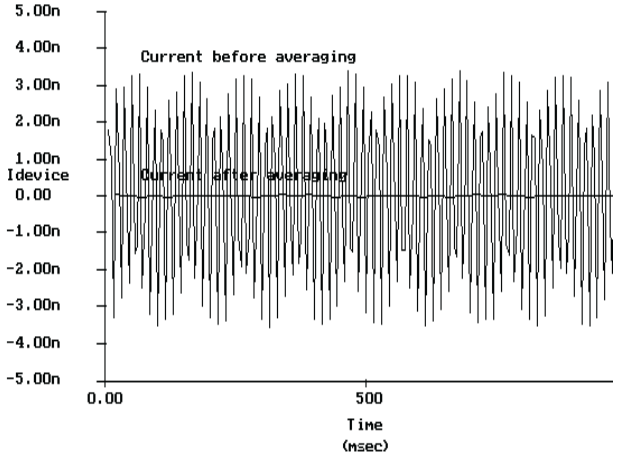

Figure 15 - Reduction of Noise Pick Up

Quick Data Without Destruction

Fast instrumentation for both acquisition and forcing simplifies the job of oxide wearout testing. Accurate timing information with uncertainties in the 5µs range means that Q_{BD} data from current and voltage ramps can be taken with timing uncertainties less than 0.5% at 1ms intervals. Thus, 200 data points could be taken within a 200ms ramp so that current or voltage resolution would also be 0.5%.

Even totaling the uncertainties, Q_{BD} could be measured and correlated to other similar platforms within 1% at high test rates. For example, a 10nm oxide could be ramped to 10V at a rate of 50V/s with step sizes of 50mV. While such speeds may be faster than the JEDEC committee agreed upon, there is ample evidence that data taken at such speeds are valid [17].

In addition to taking data rapidly, oxide wearout testing needs to be done with instrumentation which can be shut down rapidly compared to the thermal time constants of oxide test structures. If not, generated heat can fuse lines, blow out through the top of passivation structures, rapidly extrude metal leading to opens, etc.

Such failures might be obvious from visual inspection, but electrically the structures would appear open after stressing, and they might be classified as good sites.

As it only takes a few milliseconds to heat a structure to a few hundred degrees Celsius [18], the current or voltage forcing instrument has to shut down under computer control within that time. Such response times are too short for IEEE-488 bus-controlled instruments to be effective.

Driving the Chuck

It is quite common to use the wafer backside for device connection in making V-I or capacitance measurements. To do so, an ohmic contact is made to the chuck on the wafer prober which, in turn, is connected to measurement instrumentation. However, using the back side is not good practice and should be avoided if possible. Severe measurement problems are the penalty for using the chuck connection.

Instead, substrate connections should be made through probe pads on the top side of the structure with well spaced contacts so that test signals aren't compromised by contact resistance [9].

When the chuck must be used as a connection, certain steps should be followed to minimize errors:

- Use appropriate processing steps to minimize backside contact resistance without affecting the oxide under test. Failure to have good contact with the substrate results in voltage drop in the signal path, thereby delivering less than expected stressing voltage to the oxide under test. In turn, that reduction will cause an apparent voltage roll-off in the FN V/I plot and cause excessive Q_{BD} to be measured.
- Measure the chuck capacitance and resistance to ground. Then verify that the supply instrumentation can drive the impedance accurately and quickly enough for the test being run.
- Make the current measurement on the top side of the structure. The area, or antenna, of a chuck is many orders of magnitude greater than the unshielded surface area of a probe needle and probe card trace. Unless the substrate is driven with a low impedance as shown in Figure 16, noise currents (shown as Inoise) picked up by the chuck would flow into the current meter and possibly mask the tunneling current.
- Either ground the chuck or drive it with a low impedance source. Unfortunately, that may not be practical. Unless special configurations are acquired, capacitance to ground will be several hundred picofarads for a regular chuck and several thousand picofarads with a hot chuck. That type of impedance load is what often renders capacitance meter measurements impractical.

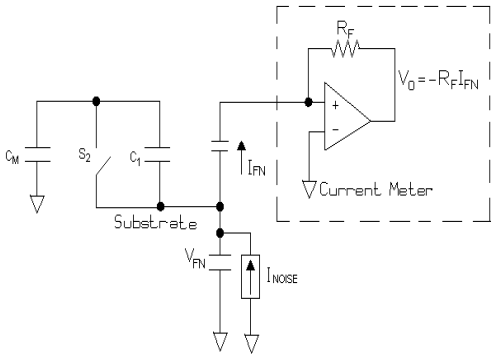

Figure 16 - Driving the Chuck

Prevent Pre-Stressing With Driven Chucks

Signals placed on the substrate are not restricted to the structure being investigated, but are coupled to all structures. That coupling makes it almost impossible to accurately determine capacitance offsets with probe cards.

For oxide wearout testing, it can also result in electron trap filling on untested capacitors. In Figure 16, the substrate is biased with the stress voltage, V_{FN}, being applied to capacitor C_1 and the resultant tunneling current, I_{FN}, is measured. A matrix/cable capacitance, C_M, is shown providing an ac path to ground. Unless precautions are taken, capacitor C_2 would also be stressed with V_{FN} times the ratio of $C_2 /(C_2 + C_M)$. To prevent such stressing, switch S_2 must be closed during the test.

Oxidized Contacts

Many materials (tungsten, polysilicon, aluminum, etc.) used for automatic probing are prone to build-up of unwanted oxidation which can cause faulty electrical contact to the device under test. In many tests (such as metal resistivity), the high impedances of oxidized contacts are readily apparent so corrective action can be taken before data quality suffers.

On the other hand, oxide test structures can mask the effect of oxidized contacts. For oxide testing, the test structure and contact oxides are placed in series so the tunneling field is divided between the oxides. Thus, the thin contact oxide has to reach its breakdown and short out before significant current can be supplied to the test structure.

One warning symptom of oxidation is having to set abnormally high compliance voltages when either forcing current or setting up a voltage ramp. However, the real problem is that breakdown of the contact oxide results in partial discharge of the cable capacitance into the test structure. That discharge is uncontrolled and can be large enough to rupture the test structure before significant Q_{BD} is measured. Thus, another symptom of contact oxidation is an excessive number of low level Q_{BD} failures despite having few shorted structures prior to the start of stressing.

Material-Dependent Noise Sources

Noise sources other than ac pick-up from nearby equipment can compromise low current measurements. While not as obvious, or as easy to independently measure, these noise sources are dependent on materials encountered in the signal path including:

- Operational amplifier current and voltage noise
- Johnson noise in the feedback resistor
- Dielectric absorption
- Triboelectric currents
- Piezoelectric currents
- Space-charge currents

Noise from the key instrumentation components (operational amplifier and feedback resistor) are thermally dependent and unaffected by mechanical motion of the other system elements. Resistance noise can be computed, and suppliers of operational amplifiers guarantee current and noise performance.

Probe Card Errors

Manually positioned probes are often used for low current measurements, but they are not practical for the high volume testing needed for effective oxide characterization. For such testing, probe cards can be built that permit precise wafer touch down with multiple pins. Benefits to test quality are many: operator errors are reduced, probing pressure is made more consistent, multiple devices can be examined with the same probing step, etc. Furthermore, probe cards can be designed to be unaffected by mechanical motion within, or near, the test system.

A major deficiency of probe cards built using conventional designs is susceptibility to dielectric absorption described later in this note. Dielectric absorption is the culprit that causes picoampere level measurements to take tens of seconds in automatic systems. As the causes of dielectric absorption lie in the printed circuit board fabrication process, and as the process is highly variable, a design solution is required that is process independent.

One solution is to completely guard signal traces against surface and bulk leakages out to, and including, the probe pins. With proper design, dielectric absorption effects can be eliminated, thereby permitting femtoamp level measurements in fractions of a second.

Eliminating Motion Detection

While probe cards and components are not usually affected by mechanical motion that is not the case for external cabling and switching systems. If those elements are not rigidly mounted to a non-vibrating platform [20], several different mechanisms transform motion to current:

- Triboelectric currents result when cable shields move relative to signal path insulation. As a result of friction, electrons are stripped from the surface layers, and the resultant charge imbalance causes current to flow until it is re-balanced. Noise can be hundreds of picoamperes with Teflon insulated cables.
- Space charge currents result from alteration of the electric field surrounding the current path. This can happen through motion of equipment or personnel. For instance, the static charge that builds up on a person from walking can be coupled to unshielded connection and cause more than one nano-ampere to flow. A ground shield common to all cabling is usually sufficient to reduce space charge effects in the cabling to femtoamp levels.
- Piezoelectric currents flow from mechanical stress within an insulator. Currents can be hundreds of picoamperes if sufficient stress is placed on cabling with excessively sharp bends, cable ties, etc.

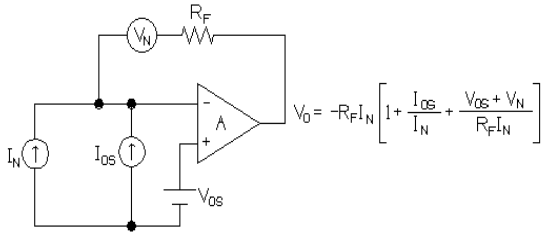

Figure 17 - Feedback Ammeter Noise Sources

The impact of errors on the ideal feedback current meter is shown in Figure 17. Calculation of V_0 provides the voltage error relative to the output; dividing V_0 by R_F results in the effective current error. Table 3 shows the span of common current noise sources which are lumped into I_N.

Current Noise (Amps)	Cables Triboelectric	Teflon Piezoelectric	Epoxy Board (DA & Leakage)	Resistor Noise (1Hz)
10^{-7}				
10^{-8}			Dirty Surface	
10^{-9}	Standard Cables			
10^{-10}				
10^{-10}				
10^{-11}			Clean Surface	
10^{-12}				
10^{-13}		Teflon		10^{9} Ohm
10^{-14}	Low Noise Cables			
10^{-15}				
10^{-16}				10^{12} Ohm

Table 3 - Magnitudes of Low Current Noise Sources

Amplification of Low Level Voltage Noise

Even with relatively low values of thermal and offset errors, low source resistance multiplies them to produce significant current errors. Table 4 was created for a picoammeter with a feedback resistor of 1Gohm, a bandwidth of 20Hz, an offset voltage of 25µV, and input thermal noise of 4µV peak to peak.

Z_{IN} (Mohms)	Thermal Noise (p-t-p) (femtoamps)	Offset Current (femtoamps)
1000	90	25
100	100	175
10	414	2153
1	4005	25000

Table 4 - Apparent Current Due to Voltage Noise

Johnson noise in the feedback resistor is computed using the relationship, $I = (4kTF/R)^{½}$, where I is the rms current, k is the Boltzmann's constant, T is the temperature, F is the bandwidth, and R is the feedback resistance. Noise gain for the offset voltage occurs according to that shown in Figure 4. Thermal noise calculations are less straightforward since Johnson noise in the feedback resistor dominates at high values of Z_{IN} and multiplication of the input noise dominates at low values.

For values of Z_{IN} comparable to the feedback resistor, thermal noise and offset current are quite acceptable. However, trying to use the range implied by the feedback resistance of 1Gohm for lower source resistance results in large errors.

Electrical Properties of Insulators

Selecting materials suitable for low current instrumentation requires good modeling of circuit requirements and thorough investigation. The best materials sometimes surprise even experienced test engineers. For instance, bulk resistivity is an important factor in achieving good low current performance, but not the most important by far. In fact, cabling with Teflon insulation has extremely high bulk resistivity, but Teflon's noise producing characteristics make it unsuitable for very low current applications.

Also, some insulating materials with the highest bulk resistivity are unacceptable due to poor dielectric absorption. In a system with active guarding, materials with lower bulk resistance may provide excellent time response and display no measurable degradation in dc performance. Table 5 provides some electrical properties of commonly used insulation materials [21].

Material	Resistivity (ohm-cm)	Piezoelectric Generation	Triboelectric Generation
Sapphire	10^{16}-10^{18}	Very Low	Low
Teflon	10^{17}-10^{18}	High	High
Polyethylene	10^{14}-10^{18}	Very Low	Low
Polystyrene	10^{12}-10^{18}	Low	High
Ceramic	10^{12}-10^{14}	Low	Very Low
Nylon	10^{12}-10^{14}	Low	High
Glass Epoxy	10^{9}-10^{17}	Low	High
PVC	10^{10}-10^{15}	Low	Low

Table 5 - Insulator Properties

Effects of Dielectric Absorption

Dielectric absorption is exhibited by even the highest quality insulating materials. Since the effects of dielectric absorption don't tend to manifest themselves except at very low currents, it is possible some of the peculiar behavior attributed (in literature) to oxides at low currents might have been due to dielectric absorption in cabling or probe cards. Because they are subtle and difficult to characterize, overcoming dielectric absorption problems is one of the most challenging tasks in building test systems capable of making high quality, low current measurements.

When dielectrics are charged to voltages within operating limits, two types of current charging are observed. One is the dominant current limited mainly by the voltage source resistance. Immediately after peak charging current is reached, it decays exponentially with time constant equal to the product of source resistance and dielectric capacitance. The other type of charging current has the same basic characteristic, but a much smaller peak value and longer duration. On close examination, it is obvious that current is not made of a single time constant. This current is called dielectric absorption because the dielectric is absorbing current well after it should have been charged.

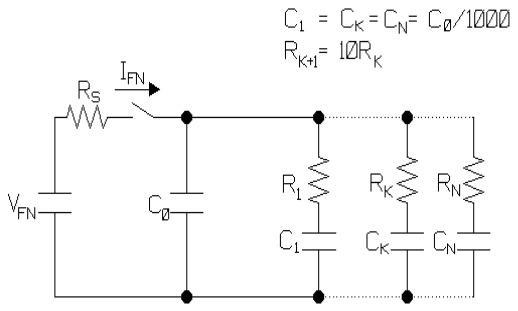

Figure 18 - Dow Capacitor Model

The physical explanation of dielectric absorption is that macroscopic dipoles are set up as a result of the migration of a few charge carriers through the dielectric. Whether in the bulk or at an interface, the trapped carriers slowly change orientation under bias resulting in very slow charging and discharging times [23].

Elegant equations with complex variables are used to predict dielectric absorption current and the variation of dielectric constant with frequency. However, in the days of analog computers, Dow [24] proposed a physical model which instrumentation designers have found useful in visualizing dielectric absorption. The Dow model is shown in Figure 18 with component values given in Hyyppa's paper [23]. C_0 is the nominal capacitance value.

As described in Equation (19), the current I_{FN} is a sum of a series of decaying time exponentials with an initial, or residual, current proportional to the charging voltage V_{FN}.

$$I_{FN} = K_0 e^{\frac{-t}{\tau_0}} + K_1 e^{\frac{-t}{\tau_1}} + .. + K_n e^{\frac{-t}{\tau_n}} \qquad (19)$$

Where:

$$K_0 = \frac{V_{FN}}{R_S},\ K_1 = \frac{V_{FN}}{R_1},..,K_n = \frac{V_{FN}}{R_n} \text{ and}$$
$$\tau_0 = R_S C_0,\ \tau_1 = R_1 C_1,..,\tau_n = R_n C_n$$

Figure 19 shows the current contributions using a five element Dow model with V_{FN} = 10V, T_n = 100s, C_0 = 500pF, and ratios from Figure 18. The linear scale doesn't provide a great deal of insight since it is dominated by the first element, but it does show the apparently linear behavior with time of the larger time constants.

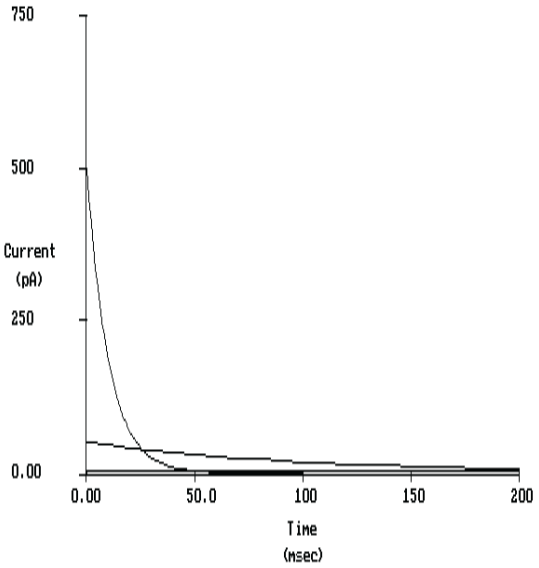

Figure 19 - Dow Capacitor Charging Times: Linear

To witness the model behavior, data in Figure 19 were transformed for viewing logarithmically in Figure 20.

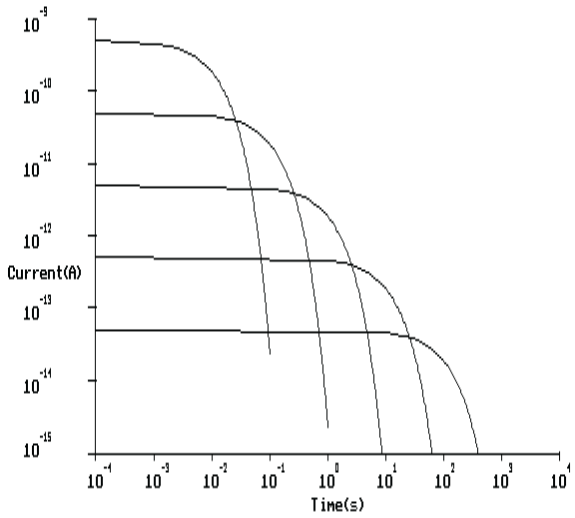

Figure 20 - Dow Capacitor Charging Times: Log

For the example given, dielectric absorption was 0.5%. That is in the range displayed by materials used as insulators. Table 6 is taken from data in Sprague and ASC data books.

Material	Dielectric Absorption (%)
Ceramic	2.50
Polyester	0.50
Polycarbonate	0.35
Polystyrene	0.10
Teflon	0.03
Polypropylene	0.05

Table 6 - Dielectric Absorption for Films

Dielectric Absorption on Probe Cards

Dielectric absorption within the probe card is one of the largest contributors and major limitations in achieving low current measurements. Unfortunately, most dc system suppliers leave probe card connection for the user. This transfers a task that is straight forward for an instrument supplier to a semiconductor engineer who seldom has the time, background, or inclination to address the problem. As a result, few systems are used for very low current measurements with probe cards even though it is virtually a necessity for low field measurements of oxides.

Problems with dielectric absorption in printed circuits are well known to low current instrumentation manufacturers. However, little reliance is placed on the insulating characteristics of through-hole plated circuit cards at low currents. Some have the design rule that any circuit connections requiring resistances higher than 1Gohms be made away from the circuit card. Thus, connections are made in the air on high quality insulators like Teflon [22] or on the surface with shielding and no path to a through-hole connection.

DA Caused by Through-Hole Plating

The problem with through-hole plated circuits is not in the base material that consists of multiple layers of fiberglass mats pressed together in a high temperature process using various binding agents. The base material exhibits high bulk and surface resistivity. However, the process of plating the through-holes contaminates internal layers with acids which leach along glass fibers and evaporate under baking to deposit salt crystals along the fibers. Those crystals act as dipoles which polarize under stress causing current flow with very long time constants. They are also the reason for reduced bulk resistivity under high humidity since moisture in the air creates a highly conductive pathway when the salts go into solution.

The amount of dielectric absorption is highly variable as evidenced by the widely varying levels of bulk resistivity reported in the literature [21] and shown in Table 5 for glass epoxy boards. Since the resistivity of the bulk material is very high, the low levels reported have to be due to subsequent manufacturing processes. Tighter process control would likely raise the lower limit several orders of magnitude above 1Gohm.

However, much higher resistivity and lower levels of dielectric absorption are of little interest to many electronic manufacturers, so there is virtually no market pressure on PCB manufacturers to address dielectric absorption and resistivity issues. That is why instrumentation companies design around the limitations of printed circuit processing.

Those design methods can be applied to the development and manufacture of probe cards for low current applications using conventional processes. Sensitivities down to 25fA have been achieved with 4 ½" rectangular probe cards built with multi-layer techniques that completely guard signal traces against surface and bulk leakages. Typical pin-to-pin leakage performance of such cards is better than 10fA/V.

Spurious Cable Charging

In addition to probe cards, consideration has to be given to the effects of dielectric absorption on shielded cables used in low current measurements. In dc parametric test systems, cable shields are typically driven with an amplifier to be at the same potential as the signal path. However, conditions exist under which the shield potential can be different from the signal path for extended periods. Thus the cable dielectric can be charged and produce dielectric absorption current when the cable is electrically connected to the current meter.

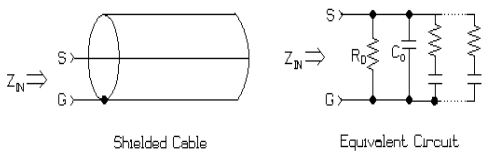

Figure 21 - Cable Dielectric Absorption Model

One common way to induce cable dielectric charging is with handling or replacement of the probe card. As the instrumentation cabling would normally be electrically disconnected during such activities, static-body voltage can be transferred directly to a signal path without benefit of a driven shield. The cable capacitance would act to reduce the imposed static voltage, but not enough. With a human body capacitance of 100pF, cable capacitance of 500pF, and static build-up to 1200V (too little to cause noticeable discharge), touching a pathway would charge it to 200V relative to a grounded shield. As shown in Figure 20, it could take minutes for the charge to completely discharge.

Spurious cable charging can also occur from overload conditions. Since instrumentation has certain voltage and current limits, seemingly normal test conditions can cause momentary overloads with little indication to the user. While such overloads are not damaging to instrumentation, they can produce bad data. For instance, using large initial voltage steps to speed up low field measurements can overload the current meter such that the shield is driven to a different potential than the signal path. On recovery from overload, the resultant discharge of the shield dielectric produces a long tail on the current measurement that appears to have a linear behavior in time.

Dielectric Absorption and Floating Meters

Although it is not a simple design task, the feedback ammeter can be implemented to measure currents away from ground. Such operation is sometimes termed “floating the meter” and is shown in Figure 22. The output current is developed across R_F and a differential circuit (not shown) is used to subtract the reference voltage, V_{FN}. For most oxide current measurements, there are few problems with floating the current meter. However, dielectric absorption effects make it quite difficult to make low field current measurements with a floating meter.

Except for very low currents, it is not difficult to address DA problems in an instrument. Of course, all contributors of dielectric absorption have to be addressed since the floating meter's reference voltage is variable. Thus, all stray capacitances internal to the meter have to be adequately shielded to prevent absorption current flow. That is not to say it can always be done. The difficulty of design is why the best low current instruments are ground referenced.

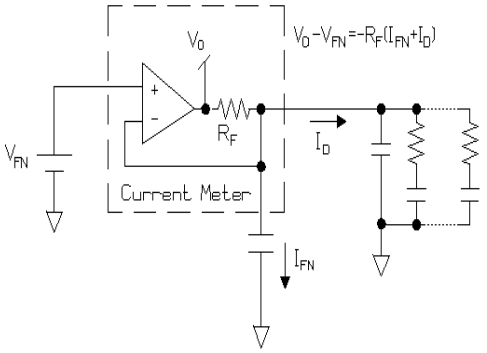

Figure 22 - Stray DA Current

The problem with DA isn't even with cabling since the shield capacitance is actively driven. The problem is with stray capacitance that cannot be shielded against. As shown in Figure 22, the voltage dropped across R_F consists of the absorption current I_D plus the desired device current, I_{FN} . The stray capacitance being charged with the absorption current is very difficult to eliminate.

The stray capacitance is also present with a ground referenced meter as shown in Figure 23, but the reference isn't continually moving and there is no signal placed across the capacitance. Thus, dielectric absorption current does not flow, and the meter measures only device current.

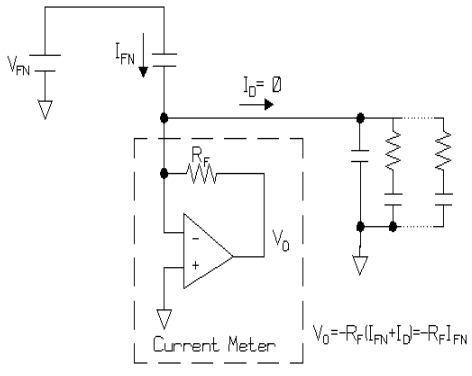

Figure - 23 Preventing Errors Due to Stray DA

Meter Overloads at Low Fields

If voltage steps applied to the oxide under test are too large, the charge transfer required to support the voltage across C_{FN} momentarily overloads the feedback ammeter. The result is a period during which the oxide capacitance is charged through the feedback resistor to a level at which the operational amplifier takes control.

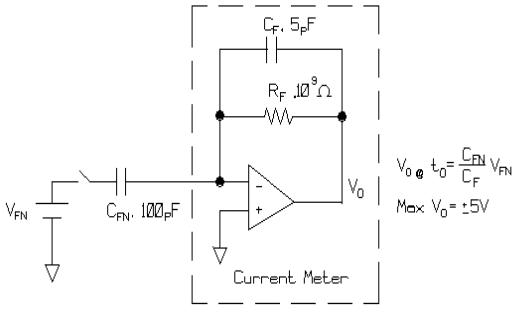

Figure 24- Model for Low Field Steps

For illustration, Figure 24 has a simplified version of a current meter with output voltage limiting, a feedback capacitance, and no input capacitance. On application of a voltage step, V_{FN} , at t = 0, the amplifier attempts to conduct all of the displacement current required to charge C_{FN} through the feedback capacitor. Since C_{FN} is 20 times the size of C_F , the output should go to 20 x V_{FN}. As long as the input voltage is less than 5V/20, or 250mV, there would be no problem supplying the displacement current. However, when the step is > 250mV, the amplifier saturates and some of the displacement current has to flow through the feedback resistor, R_F. For this example, that time constant is equal to R_F x C_{FN} or 100ms. That is quite long compared to the 5ms time constant of the feedback network.

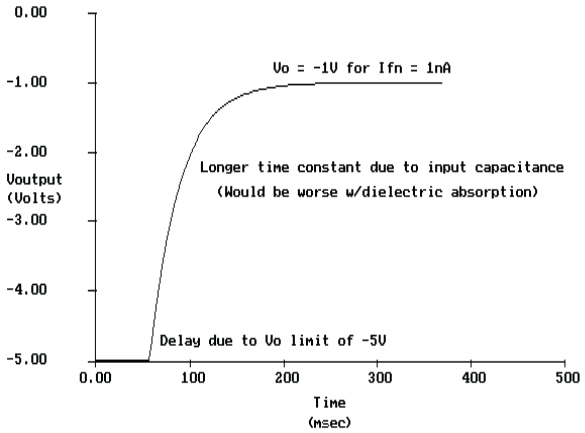

Figure 25 - Overload Recovery to Step

The larger the voltage is above 250mV, the longer it will take to discharge to near zero volts where the amplifier can re-assert control. The result of a 10V overload is shown in Figure 25. Although it would be significant in practice, no attempt is made to show the absorption current which would flow from the cable dielectric and might take several minutes to effectively disappear.

Industry Standards and Practice

Industry standards for both Jramp and Vramp testing have been proposed by JEDEC, but each has some deficiencies. Certain modes of failure are not detected and can lead to invalid results for Q_{BD} [25].

- For instance, a failure while under Jramp testing might not cause an immediate drop in device impedance even though the test structure is no longer a capacitor. If the resistance of the failed device happened to conduct a fraction of the tunneling current, it would go undetected until another location within the same structure did fail with a short of low enough resistance to cause a significant drop in voltage. Excessive Q_{BD} would thus be reported, and that is why using a percentage voltage drop to indicate failure sometimes produces invalid data.
- The same type of failure might be missed with the Vramp test if the resistance is equal to the voltage - current ratio at breakdown since the failure would not cause an appreciable change in current flow.

Data-Based Testing

A data-based test environment simplifies experimentation for the technologist investigating oxide reliability. Software architectures can be designed which permit interactive test setup, editing, and immediate testing without having to recompile or execute an interpretive programming language. By using a compiled data-based test program, interactive mode testing is exactly the same as when operating at full speed.

Furthermore, compiled software improves the data quality process. Code can be maintained at much higher quality because fewer programmers actually make code changes. Instead of changing or writing code, other system users concentrate on using the data base software. Problems with the code go through a formal review process prior to implementation.

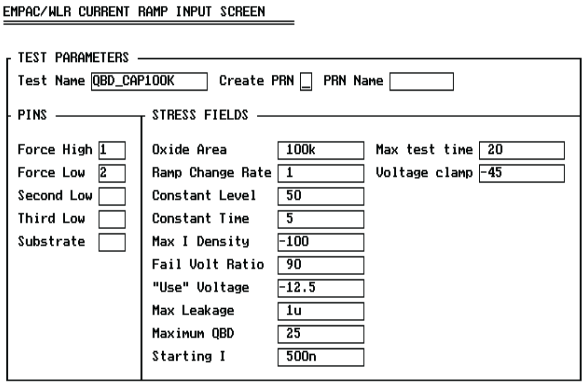

Figure 26 - Input Screen for EMPAC Jramp

In the same way that data bases, word processors, and spread sheets have improved communication among diverse work groups, data-based test software improves communication among users of test structures. Furthermore, if the data base software is acquired from a commercial supplier, non-proprietary communication about test structures can extend beyond the company's boundaries.

Without the standardization that data-based software delivers, even those engineers using the same test platform often diverge under the pressure to make changes so that desired results are achieved.

In the noise graph of Figure 15, the data-based EMAGE (Electrical Measurements for Analysis, Graphing, and Evaluation) software was used to change initial delays, delays between readings, digital integration integer, etc. without having to re-compile and/or look at source code. Besides noise rejection and timing inputs, failure criteria, activation energies, and other device descriptors should be adjustable. Figure 26 shows one input screen for the EMPAC (Electrical Measurements for Process Analysis and Control) WLR Jramp screen.

Summary

Test instruments and systems are important elements in a data creation process. That process starts with sound test structures and is not completed until actionable data are created. Inputs to the data creation process can be identified, measured, and their effect created. Test systems do not have to be treated as magic boxes.

While characterization and modeling of ATE systems and fixtures is simple compared to that encountered in semiconductor manufacturing, creation of high quality oxide wearout measurement systems requires diligent investigation, extensive experimentation, and good design practices.

Conditions under which published specifications apply have to be considered so that data from instrumentation can be trusted and turned into information. The cost of not understanding performance limits is data which have to be evaluated and censored before action can be taken. By proper modeling of static and dynamic effects, low level measurement errors can be bounded, thereby providing the means of predicting performance through the entire range of oxide wearout testing.

Properly addressing the error contributors identified in this note can result in fast, effective test systems which can be built without reliance on exotic techniques and materials. Naturally, Reedholm dc parametric test systems, probe cards, and probe card fixtures exemplify such systems.

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