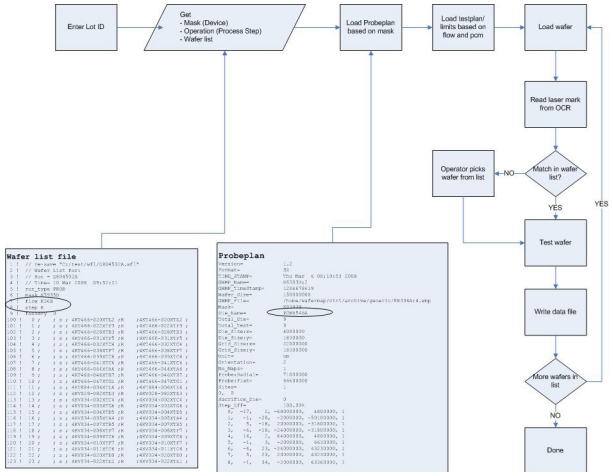
APPLICATION NOTE

AN-128

Compound Semi - Wafer Level Testing

I) Introduction

Reedholm dc test systems are used by a large number of GaAs and other compound semiconductor foundries in a variety of roles. These systems are used by both manufacturing and engineering departments. They offer a high degree of automation in the area of data acquisition, as well as providing network access allowing engineers to work more efficiently.

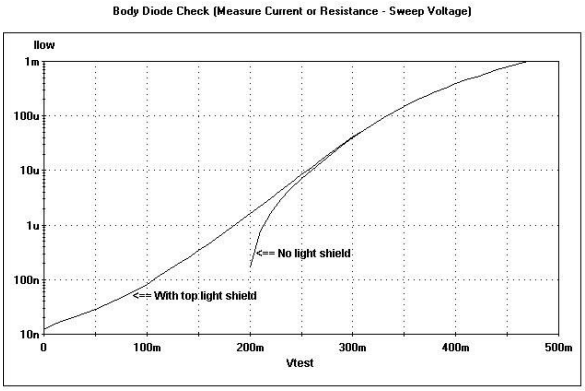


The following applications descriptions illustrate how our measurement tools might be used in your operation. For each, requirements unique to high gain and high power devices have been addressed:

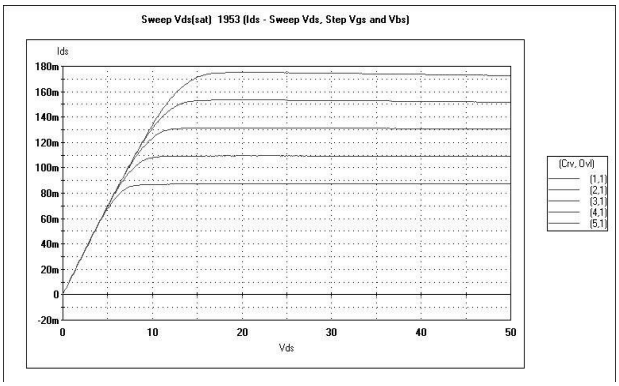
- Sensitivity to Damage – Special instrumentation power-up and power-down sequencing is incorporated in the test code.
- Propensity to Oscillate – While needing to be solved at the test fixture, the analog cables and probe cards provided have proven to be well suited for the addition of ferr-magnetic mats, ferrite beads, and/or discrete components for the reduction of transistor oscillation.
- Possibility of Self-heating – High current instrumentation beyond the standard 550mA is available, providing extensions for both 5A and 50A requirements. Pulsed measurement techniques also help prevent excessive heating.

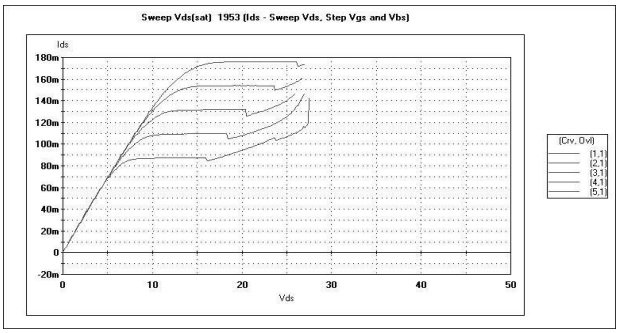
II) Device Characterization

Delivered standard with all Reedholm systems is a built in curve tracer. This makes it possible to look at comprehensive I-V characteristics, inclusive of analog cabling and probe cards, thereby simplifying the task of correlating results to production. Below is one such plot detailing measurement effects with and without a light shield:



This curve tracing capability is quite helpful when trying to identify and resolve sources of device oscillation. For example, the curve tracing capability makes it easy to see and quantify the difference in results with and without an added capacitor.





III) Process Control

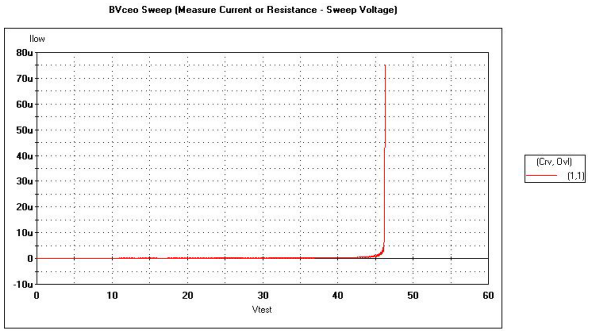
Routine measurements of process control monitors, both in-line and end-of-line, provide feedback to the process engineers about the manufacturing flow. Whether for GaAs processes or those for HEMT devices and BJTs, Reedholm comprehensive applications environments and precision instrumentation provide the test coverage needed by even the most stringent requirements.

Test algorithm coverage includes measurements of:

- Ohmic contact resistance
- MESFET characteristics (Idss, Gm, pinch-off, etc.)
- Transmission line characteristics
- BJT characteristics (Gain, breakdowns, early effects, etc.)
- Mesa Resistor,Isolation, and Gate Etch Characteristics
- Interconnect resistance
- Various types of capacitors

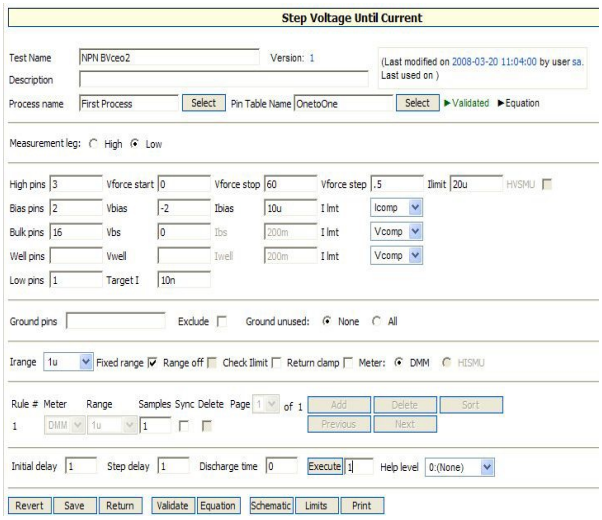
IV) BVceo Measurement Flexibility

To illustrate the flexibility of the algorithms, several ways of measuring BVceo are shown, each with advantages and disadvantages. Four techniques are reviewed below use 10uA as the targeted collector-emitter breakdown current. Prior to investigating the various techniques, a sweep of V_{CE} was done while measuring I_C with the base pin floating to find that the real value for BV_{CEO} was 46.35V.



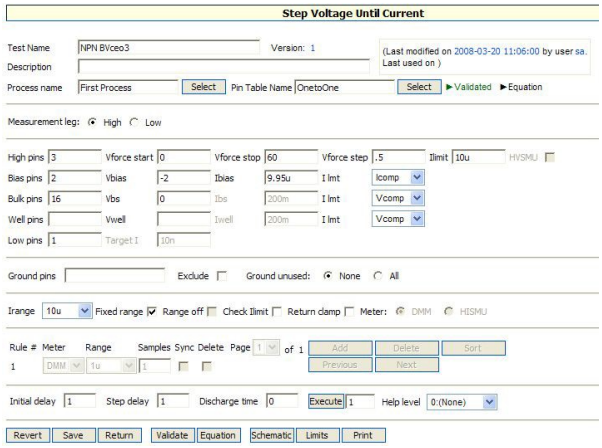
A) Force 10uA, Measure V_{CE}

The first technique forces I_{CE} and measures V_{CE} after sufficient delay, and with the base pin floating.



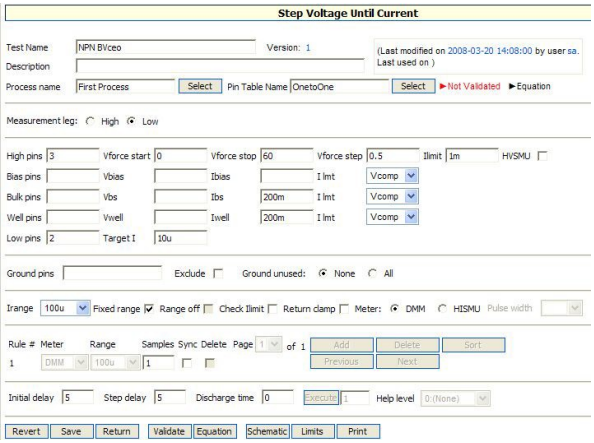
B) Step V_{CE} Until I_{CE} Reached

The second technique steps the collector voltage until the target collector-emitter is measured, again with the base pin floating.



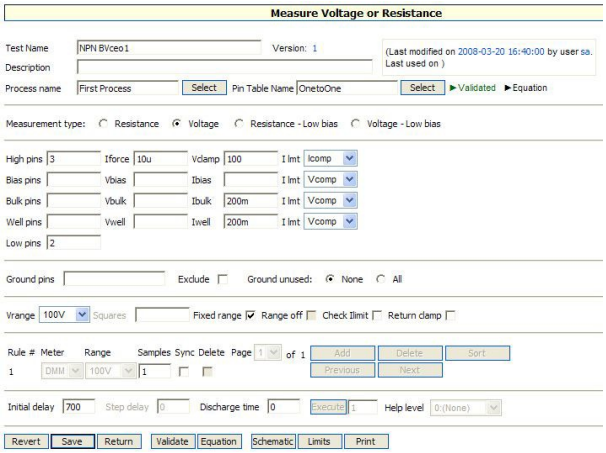
C) Step V_{CE} Until $I_{B.}$ Reached

The third technique forces 10A and steps collector voltage with >>10uA limit until base current changes polarity (e.g. 10nA).



D) Step V_{CE} Until I_{CE} Reached, Grounded Base

The fourth technique has the base grounded, and forces 9.95uA in the emitter and steps the collector voltage until 10uA is reached. Note that the measurements are made in the high lead during this test.



E) Summary of Results

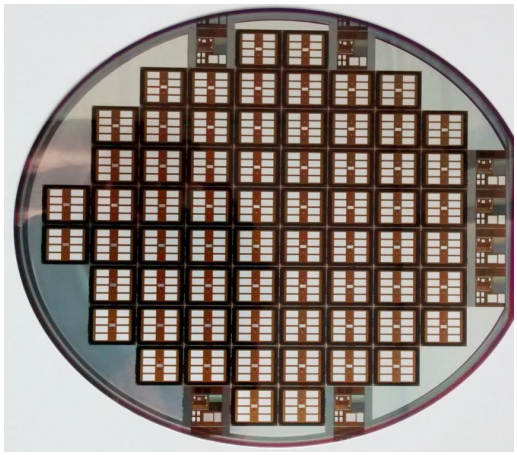
The table summarizes the results for four ways of measuring BVceo and complete test times:

Test	BVceo	Test Time
Force 10uA, Measure VCE	46V	650msec
Step V_{CE} Until I_{CE} Reached	46V	768msec
Step V_{CE} Until I_{B} Reached	47.5V	268msec
Step V_{CE} Until I_{CE} Reached, Grounded Base	47V	395msec

V) DC Sort & Functional Test

Before the start of full-wafer testing, wafers can be subjected to a dc functional test on a subset of the product die. Potential wafer yield can be calculated and decisions made as to the quality of the remaining product die. Reedholm's testing applications make it easy to create and execute different probing patterns using common test sequences.

When shown to have an acceptable yield, all die on the wafer are tested with die status stored electronically and/or indicated by inking the malfunctioning die.



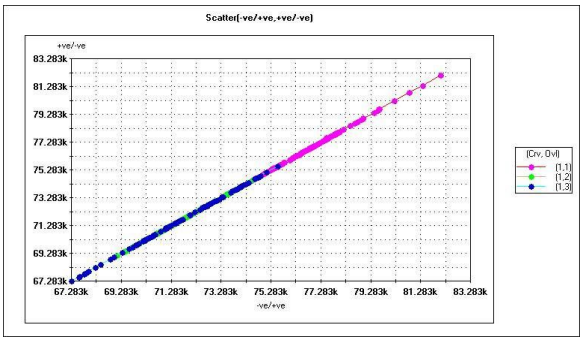
When stored electronically, data files can be used later by visual inspection as well as pick and place equipment. Features exist in the testing application so that inking can be done at or behind the site being probed, as well as off-line after testing. Software support also exists for testing portions of wafers which contain multiple products.

Key to dc functional test, where potentially thousands of die require testing, is test execution speed and equipment costs. Not only does the reasonably priced Reedholm test instrumentation provide superior throughput to IEEE-488 controlled instrumentation and other alternatives, the applications software allows easy test sequence optimization.

Test Name	Last Result	Test Time	Average	Minimum	Maximum	StdDev
Iges+ Vge=20V	190.257p	188m	283.884p	189.319p	490.464p	98.81p
Iges+ Vge=30V	481.082p	188m	477.236p	301.896p	652.763p	112.275p
Iges- Vge=30V	-573.394p	188m	-718.338p	-844.519p	-573.394p	80.3396p
Iges+ Vge=50V	1.68566n	190m	1.29877n	982.053p	1.68566n	184.228p
Iges+ Vge=21V	102.071p	188m	248.328p	102.071p	390.082p	103.07p
Vge(th) Ic=15uA	4.98735	21.9m	4.98751	4.98704	4.98954	754.737u
Vge(th) Ic=5mA	5.83482	19.3m	5.83473	5.83451	5.83514	210.915u
Vge(th) Ic=2A	7.14168	62.3m	7.14228	7.14136	7.14673	1.60421m
Gain Vth	5.21065	671m	5.21056	5.21026	5.21065	110.675u
Gain Vgs	5.5	44.5u	5.5	5.5	5.5	0
Gain Ids	350.259u	43.9u	350.371u	350.259u	350.921u	196.073n
Gain Calculation	4.18349m	204u	4.18233m	4.18019m	4.18349m	946.58n
Vce(on) Ic=50A	2.35544	72.1m	2.34962	2.33128	2.36168	8.82151m
Ices[EHT] Vce=100V	222.751n	125m	160.743n	104.012n	222.751n	45.4346n
Ices[EHT] Vce=1000V	258.02n	197m	240.157n	209.871n	258.02n	15.9454n
Ices[EHT] Vce=2000V	308.418n	196m	296.789n	272.327n	308.418n	10.8469n
Total	-	2.30689	-	-	-	-

Optimization alone can provide a doubling or tripling of die tested per hour, reducing the need for additional test and probing systems. Other test time reduction features include the possibility to skip to the next die as soon as a critical parameter's failure is detected, as well as several options relating to the frequency of test data storage.

VI) Analysis of Results



In addition to the tools previously described, the software includes an automated means of providing an array of summary data:

- Histograms to look at data distributions
- Scatterplots to evaluate relationships between test types or results
- Wafer maps to evaluate uniformity across a wafer for a given set or sets of parameters
- Reductions and trend charts to evaluate results over time.

VII) Training, Installation, and Ongoing Support

Comprehensive training, installation services and ongoing support are available. Also available are reasonably priced service agreements that make it cost effective to control operational expenses as well as providing long term access to technical support for answering questions and helping to resolve problems.