WLR Test Routines

- **Sensitive to Known Physical Phenomena**
- **Careful Control of Stress Variables**
- **Primary Failure Mechanism Promoted**
- **Shortest Possible Test Times**
- **Test Structure Characterization Built-In**

When used with Reedholm fast WLR test structures, these WLR test routines rapidly accelerate targeted failure mechanisms. The unique attributes of RI series test systems minimize timing uncertainties and provide high power levels where required. The algorithms comply with standards set by the JEDEC subcommittees and can also be used on structures not developed by Reedholm.

Test Types

Test algorithms include standard EMPAC test menu choices, WLR choices, or a combination of each. Table 1 contains the list of routines available.

Test Routines	
SWEAT EM	Contact EM
Isothermal EM	Mobile Ion/SOG Charging
Constant Current EM	BEM
Via Voiding	Jramp

Table 1 - Reedholm WLR Test Routines

Test Results

With most dc tests, a single output is desired. This is not the case for most WLR tests. Along with stress/test duration, WLR algorithms return additional information that is test specific, including:

- Temperatures
- Resistances
- Cumulative Charges
- Voltages
- Currents

The reason for test termination is returned as the result category. These are unique to each WLR test type. When test conditions are properly selected, and test structures behave as predicted, the expected result category is returned.

Following is an example of results available when executing thin oxide reliability tests:

- Ramp duration
- Q_{BD}
- Final measured voltage
- Final forced current
- Ratio of calculated to actual test duration
- Use voltage
- Pre-ramp leakage current at use voltage
- Ramp multiplier
- Initial current of the ramp
- First voltage during constant current stress
- Last voltage during constant current stress
- Slope during constant current stress
- Maximum voltage during constant current stress
- Minimum voltage during constant current stress
- Result category (Table 2)

#	Result Category
0	Test did not start.
1	Reached allotted time without failure.
2	Reached current compliance without breakdown.
3	Exceeded breakdown current at first ramp point.
4	Reached maximum Q_{BD} without breakdown.
5	Reached voltage compliance without breakdown.
6	Reached breakdown, but did not stay shorted 6.1 - Shorted, indicated by DMM overrange.* 6.2 - Current exceeded max. value entered.* 6.3 - Slope exceeded max. value entered.* 6.4 - Negative slope - decrease in current.*
7	Did not reach breakdown, but is shorted.
8	Reached breakdown and stayed shorted (desired) 8.1 - Shorted, indicated by DMM overrange.* 8.2 - Current exceeded max. value entered.* 8.3 - Slope exceeded max. value entered.* 8.4 - Negative slope - decrease in current.*
9	Initial current leakage was excessive.
12	Reached maximum number of data points.

Table 2 - Result Categories

Key Advantages

Timing Accuracy

Unlike most dc parametric test applications, highly accelerated WLR testing requires tight timing control for data acquisition. A single tasking MS-DOS based computer is a first step towards full control. Multi-tasking computers inject too many uncertainties for effective, precise time control. Real time clocks that address timing are inadequate for high speed ramps. The timing overhead to service them is too great.

For optimum noise rejection in dc test applications, Reedholm enhanced the crystal controlled PC clock with machine code, providing timing measurements with 45µs uncertainty. Thus, precision Q_{BD} measurements can be made with much more accuracy than is possible using alternate techniques.

Instrument Control

Rapid control of a dc test system's instrumentation is critical for test throughput. For WLR testing, it can even be vital for accurate test results. Reedholm's proprietary computer interface card (CIC), in combination with today's high speed personal computers, allows instrument register data transfer in less than 4µs. For reliability testing, this high transfer rate can shut down a stress power source before undesired damage to the test structure occurs. Other test types use this speed advantage to make smaller steps in voltage and current ramps, while maintaining the desired ramp rate. Smaller steps effectively increase the test algorithm's resolution and accuracy.

High Current Stress

Design of Reedholm's voltage forcing/current forcing (VFIF) programmable power supplies allows them to be used in parallel. This capability is used by several metallization tests where high stress currents are required. It is also used by self-heated and poly-heated structures, where the output of a single supply would limit temperature span. For applications requiring stress currents between 550mA and 2A, an external IEEE-488 controlled current source is available.

High Voltage Breakdown

Most dc test systems' standard voltage sources are limited to 100V or 200V. That is not enough to find hillock or cracking problems with a typical intermetal dielectric (IMD). For such thick oxides and insulators, thinning cannot be detected using Fowler-Nordheim tunneling until the hillock has virtually grown through the insulation or the crack is extremely severe.

Reedholm has solved this limitation with a high voltage option that provides production worthy 1500V wafer level measurements. Thus, IMD's up to 1.5µm can be monitored with proper probe card setup. The self-calibrated high voltage option provides breakdown measurements with uncertainties <0.1%. Resistance of 100kΩ is placed in series with the high voltage output to minimize effects of energy storage in the cable. All high voltage connections are made with non-corona wire.

Figure 1 shows the difference in breakdown characteristics making IMD measurements difficult.

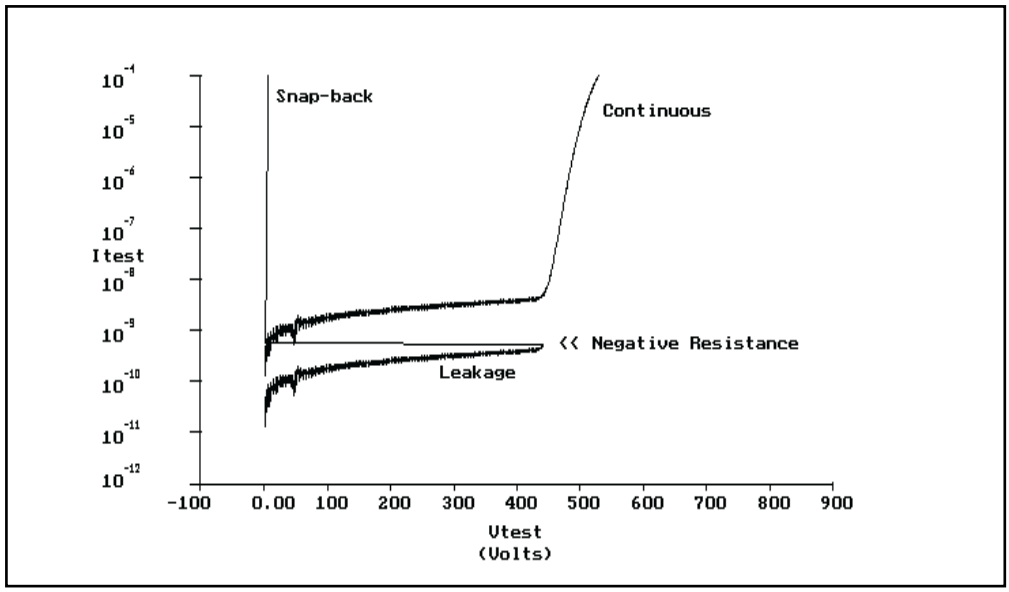

Figure 1 - Breakdown Characteristics

Software Subsections

Test Set-Up Screen

WLR tests are simple to create, and require no additional programming. When an EMPAC WLR test type is selected, the test set-up screen automatically displays. Stress and exit criteria cells displayed on the right side are populated with default answers. A brief cell explanation is provided, inclusive of the units used and range of valid responses. The validity of an individual cell is checked when exiting the cell. Invalid cell entries are flagged. A help line above the grid explains each cell on the input screen when it is active.

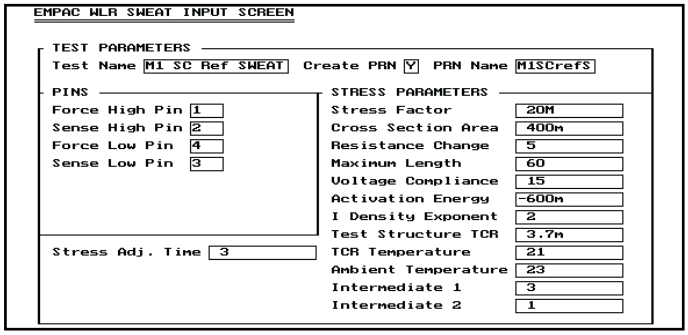

Figure 2 - Metal Step Coverage Test Setup

Test Feedback During Development

During execution, metalization and self-heated tests provide intermediate values of temperature, resistance, current, etc., which are displayed on the bottom of the PC's monitor. Immediately after the test, a full-screen display is provided, listing most relevant test information. Oxide testing with Vramp and Jramp also provides initial timing measurement information prior to start of test. Figure 3 shows output to the screen at completion of the Vramp TDDB test when used in the engineering structure characterization mode.

```
                REEDHOLM RAMP TEST RESULTS
          ************************************

Actual Time      =   1.0397E+01   Constant Time   =   0.0000E+00
Data Points      =   554          Time Ratio      =   9.8949E-01
QBD: Cum Charge  =   4.4003E-04                   =
Final Stress     =   5.8700E-04   Final Stress V  =   1.8800E+01
Result Category  =   8                            =
Ramp Step Size   =   2.5000E-02   USE Voltage     =   5.0000E+00
Initial Leakage  =   1.2867E-09   Final Voltage   =   1.0000E+20
```

Figure 3 - Vramp TDDB Test Output

Graphical Engineering Outputs

For WLR tests without an equivalent test type in EMAGE, test algorithms generate data files with measured and calculated data. Plots of temperature, cumulative charge, resistance, etc., vs. time are available for viewing in EMAGE, depending on test type.

Figure 4 is representative of the type of plots generated by the SWEAT EM test in the engineering characterization mode. Note the rapid rise to the desired acceleration without current or temperature overshoot.

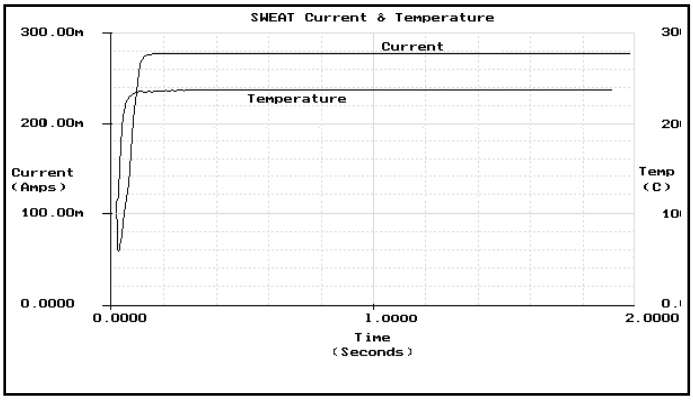

Figure 4 - Typical SWEAT EM Test Plot

Error Trapping

Error trapping is at the core of each Reedholm data acquisition package. It assures the integrity of instrumentation and software so that system crashes are eliminated and erroneous test results are flagged. In essence, robust operation is provided with test algorithms that:

- Check possible errors
- Prevent data corruption/cessation
- Compare with decision making criteria
- Take corrective action as required

Each WLR test type has structure integrity checks that determine whether test execution should continue. Should a structure fail an integrity test, the nature of the problem is returned in the form of an encoded error number. This pre-check for open or shorted structures not only saves valuable test time, but prevents execution errors that could occur attempting unrealistic stress conditions.

Table 3 is an example of the encoded errors for one of the self-heated algorithms.

#	Encoded Error Descriptions
1	Not used.
2	Element being biased appears shorted.
3	Error in measuring temperature.
4	Cannot force the current to reach 100mV on the DUT.
5	Not used.
6	Do not have the third VFIF required.
7	Temperature monitor appears open.
8	Not used.
9	Not used.
10	Heater element appears open.
11	Not used.
12	Not used.
13	Not enough heap for the PRN arrays.

Table 3 - Encoded Error Descriptions

Documentation

Complete documentation is delivered with the WLR test routines, covering:

- Test sequence overview
- Test structure considerations
- Complete test description
- Schematic set-up screen
- Cell descriptions
- Post-test screen description
- Test results available
- Encoded error definitions
- EMAGE plots created

Figure 5 is an example schematic for sodium contamination testing.

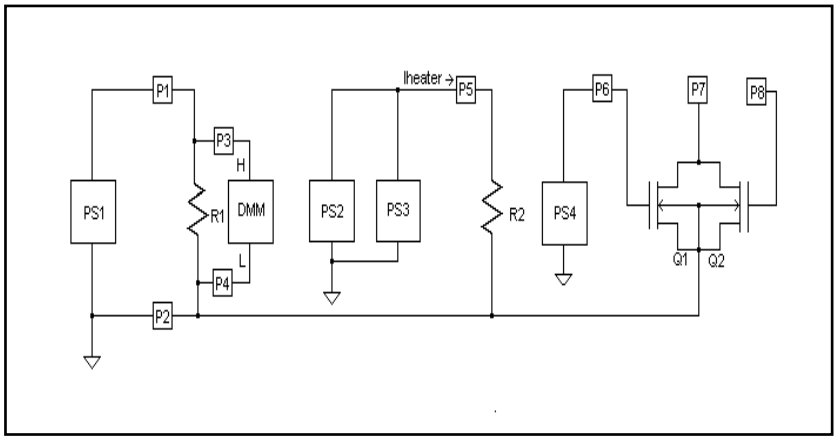

Figure 5 - Sodium Contamination Test Schematic