

Reedholm Distribution Software: The RDS Intranet Editions

- **Test Plans and Results in SQL Database**
- **Test Documentation & Version Control**
- **Integrated Analysis & Lot Reports**
- **High Volume Automatic Probing**
- **Multi-mode Data Export**
- **Simple Fill-in-the-Box Test Editing**
- **No Source Code to Maintain or Compile**
- **Integrated Curve Tracer (I/V, C/V, I/T, V/T)**
- **Built-in Throughput Optimization**
- **Self Test & Troubleshooting Tools**

Introduction

Twenty years of experience providing dc test solutions were incorporated in RDS Intranet when it was first released in 2003. It provided a comprehensive dc test suite that improved yield team productivity, expanded test coverage without throughput loss, and made it easy to resolve test issues. After seven years of continual improvement, RDS Intranet is even better.

Unlike other parametric test environments, RDS Intranet is a WEB application running on top of Microsoft SQL Server. This means that all information related to dc test is stored in a database: test routine parameters, probe patterns, lot test results—even the application user interface text, which can be customized per user. It also means that RDS Intranet can be accessed from any Windows PC with Internet Explorer, expanding the reach of dc test throughout a company without requiring a team of IT personnel. Access to the database has multiple levels. For instance, those responsible for parametric test might be granted full rights, design engineers would have read-only access, and operators might only interact with workflow data.

Even more important than the convenience of being a WEB application is the virtual elimination of writing, compiling, and maintaining source code without surrendering flexibility. Each test type in table 1 has dozens of input fields (many of them optional), so each test input screen is equivalent to dozens of routines in a typical test library. Thus, the RDS Intranet test engine is equal to a test library with 100's of source code routines written in Basic, C++, or Fortran.

2 Terminal Resistance - Force Current or Voltage
3 Terminal Voltage or Resistance
4 Terminal Voltage, Resistance, or van der Pauw
Beta at an Ib, Ic, or Ie
Calculate Delta Length
Current at a Voltage
Early Effect
gm or Vt at an Ids or % of Ids
gm or Vt at 2 Ids, 2 Vgs, or PMS
High Voltage (+2kV) Continuous & Snapback BV
Ic - Sweep Vce, Step Ib
Ic - Sweep Vce, Step Vbe
Ic and Ib - Sweep Vbe
Ids - Sweep Vds, Step Vgs and Vbs
Ids - Sweep Vgs, Step Vbs
Ids - Sweep Vgs, Step Vds
Ids at a Vgs
Isub - Sweep Vgs, Step Vds
Measure Capacitance at 0V, ±100V, or +2kV
Measure Capacitance – Sweep ±100V or +2kV
Measure Current or Voltage
Measure Current - Sweep Time
Measure Current - Sweep Voltage
Measure Current at High Voltage (+2kV)
Measure Resistance - Low Bias
Measure Resistance - Sweep Voltage
Measure Resistance at Current
Measure Resistance (4T) – Sweep Current
Measure Resistance at Voltage
Measure Voltage - Low Bias
Measure Voltage – Sweep Time
Measure Voltage (4T) – Sweep Current
Peak Beta
Replace Test Parameters with Prior Results
Saturated Vt
Small Signal Beta
Standalone Equations & SQL Extractions
Step Voltage Until Current
Stress at a Vgs
Stress Current
User Written Test
Vgs at an Ids, % of Ids, or Peak Isub
Voltage at a Current (±100V or +200V)

Table 1 - Subset of Available Test Types

Thousands of Test Variations

Callouts in this RDS Intranet input screen are representative of the richness for each test type. In addition, equations can be added to each test or function as stand alone tests. Complex extractions such as least squares fit on I-V or C-V sweeps can be performed in real-time.

gm or Vt at Two Gate Voltages

1) Test Name: ECR Schem - Gm @ 2 Vgs Version: 1 (2) (Last modified on 2009-12-28 11:10:00 by user sa. (3) Last used on)

Description: Example test routine

Process name: CMOS Select Pin Table Name: OnetoOne Select ▶ Not Validated ▶ Equation (4)

5) Transistor type: N-type P-type Measurement leg: Drain Source (7)

6) Return type: gm Vt

Drain pins: 8 Vds: 100m I_{ds}: 1m I_{lim}: Vcomp HV: (8)

Gate pins: 2 1st V_{gs}: 2 2nd V_{gs}: 3 I_{gs}: 1m I_{lim}: Vcomp

Bulk pins: 3 V_{bs}: 1.1 I_{bs}: 10m I_{lim}: Vcomp

9) Well pins: 4,23 V_{well}: -5 I_{well}: 1m I_{lim}: Vcomp (11)

Source pins: 1 (10)

12) Ground pins: 6,7 Exclude: Ground unused: None All (13)

14) I_{range}: 100nA Fixed range: Range off: Check limit: Meter: DMM PAM HISMU Pulse width: 300u (16)

17) Rule # Meter Range Samples Sync Delete Page 1 of 1

Rule #	Meter	Range	Samples	Sync	Delete	Page
1	DMM	1u	10	<input type="checkbox"/>	<input type="checkbox"/>	1 of 1
2	DMM	100nA	1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	1 of 1

18) Discharge time: 0

19) Initial delay: 5 Step delay: 1 Discharge time: 0 Enable BKD: Execute: 1 Help level: 0:(None) (21)

20) Execute: 1

22) Revert Save Return Validate Equation Schematic Limits Print Prev Next Move to: ECR Schem - Gm @ 2 Vgs (26)

Figure 1 – Input and Edit Test Grid

- 1) Brief description field for each test.
- 2) Built-in version control allows one version to be released to production while a new one is debugged.
- 3) Test edits and usage automatically tracked.
- 4) Flag indicates if test has attached equation.
- 5) Transistor type adjusts voltage polarities.
- 6) Selects return parameter, with other returned in memory array so test doesn't have to be run twice.
- 7) Select leg in which measurement is made.
- 8) Directs usage of optional HV bias ($\pm 250V$ or $+2kV$).
- 9) Fifth device pin assignment can be biased. Up to 12 pins can be assigned for each of six pin fields.
- 10) Values can be engineering notation (1m, 2k, etc.).
- 11) Extra pin biasing can force voltage or current.
- 12) Pins to ground or exclude from grounding.
- 13) Single input to ground all unused pins.
- 14) Set starting range for faster testing, fixed range or not.
- 15) Power down during range changes to protect sensitive devices and make sure supply is in correct mode.
- 16) Standard or optional current meters (low or high).
- 17) Ranging rules assure the right answer in shortest time.
- 18) Eliminate line frequency 60/50Hz noise.
- 19) Separate delays for initial bias and bias between steps.
- 20) Loop on test to gather optimization timing data.
- 21) Increase help to investigate test issues.
- 22) Validation to ensure proper test execution.
- 23) Launch equation editor to manipulate test result.
- 24) Obtain schematic of instrumentation connections.
- 25) Launch editor to set or modify test limits.
- 26) Quickly move between tests during editing.

Testing without Spawning Code

RDS Intranet does not spew out test code in C++ or some other language that the test engineer has to tweak and maintain forever. Instead, dozens of fields in a database record are populated when setting up a test. That record is downloaded to a test controller and executed in real-time without any delays for compiling.

Setting up and controlling test plans is similar to populating spreadsheet files. Flexibility is more than adequate, so the language used to write the application has no bearing on the work product. All that matters is getting results that make sense and that can be easily verified when there are yield problems.

Out Sourcing the Test Engine

Instead of a user interface and a handful of example test routines, RDS Intranet contains a comprehensive set of test routines that cover bipolar, depletion FET, and enhancement FET technologies implemented on Si, GaAs, GaN, and SiC materials. Years of experience supporting customers at the application level has resulted in a robust, fast, and flexible test engine that can be used immediately for test plan generation.

Compare that to test engineers having to learn how instruments, analog cabling, source code, and operating systems interact just to create a test library from which test plans can be written. But getting a test engine going is more than writing a test library. These are just a few of the other RDS Intranet features that would be needed:

- Prober driver and probe site editor
- Lot reports and test data exporting
- Version control of test library and plans
- Test routine code documentation
- Test conditions (pins, voltages, etc.)
- Training for test engineer replacement

As difficult and expensive as in-sourcing is with an integrated tool set, doing it with a rack and stack configuration is significantly more difficult since the various instrument, cabling, and computer combinations have to be characterized.

More Than a Set of "Canned" Routines

"Canned" source code routines provided as examples lack the ability to test many device permutations, and that is why source code has to be customized. However, the RDS Intranet test engine supports:

- Multiple pins per DUT leg (drain, gate, etc.)
- Biasing and grounding extra DUT pins
- Forcing voltage or current on extra pins
- Executing user input equations
- Using prior test results for test conditions

After a test is created and found effective, being in record format makes it easy to copy and use as the starting point in setting up a new test.

No Test Engine Ambiguity

Suspect test data is sometimes caused by improper test conditions or incorrectly selected algorithms. Reedholm software algorithms are not subject to uncontrolled tweaking, so valuable time is not spent trying to work backwards through code changes. Furthermore, since all test conditions are stored in a centralized, controlled database instead of being hard code, there is no ambiguity over what was used during testing. Lastly, automatically generated test schematics (figure 2) illustrate how the test conditions and algorithm interact.

So, when test problems are encountered, device engineers totally unfamiliar with Reedholm software, but armed with critical device knowledge, can contribute directly in problem solving.

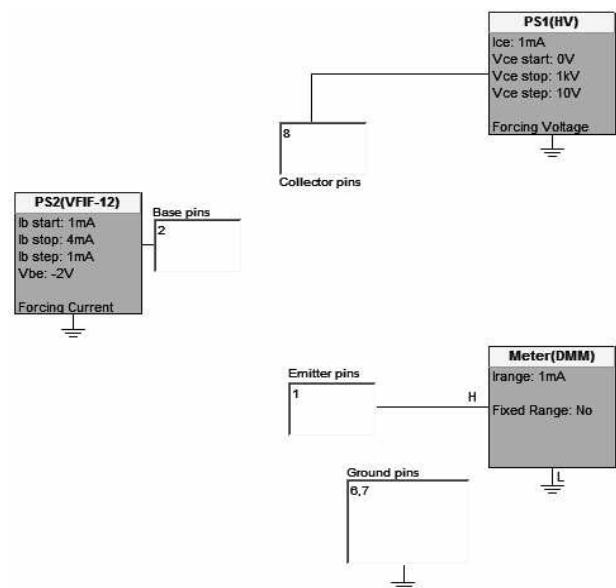


Figure 2 - Schematic Generator

Integrated Device Characterization

RDS Intranet allows it to perform as a curve tracer. It is not necessary to take a wafer to another station to generate characteristic curves like the bipolar transistor curve in figure 3 and the MOSFET curve in figure 4.

Properly used, this capability eliminates uncertainty about device behavior and what test conditions to use to assure the highest quality data. A curve, or set of curves, can be created for almost every test type listed in table 1.

No Compromise on Test Speed

The flat, memory mapped architecture used by RDS Intranet for system control is inherently faster than what is possible with multiple instruments, each having processors for control. Test code execution speed is as fast as the most optimized version of compiled code. Data driven testing is sometimes misinterpreted as having an interpreter level. But that could not be further from the truth. Data is not moved or modified during software execution, so speed is the same as if data were compiled with the code.

Delays and result averaging to reduce noise are the major reasons for slow testing. Those creep into compiled routines, and programming engineers never seem to have time to take them out. With Reedholm software, delays and averaging are selected with as much flexibility as needed to match what is found with response versus time plots unique to Reedholm.

After a test plan is set up for volume testing, reports like that in figure 5 are generated to identify test speed bottlenecks to review for further speed increases.

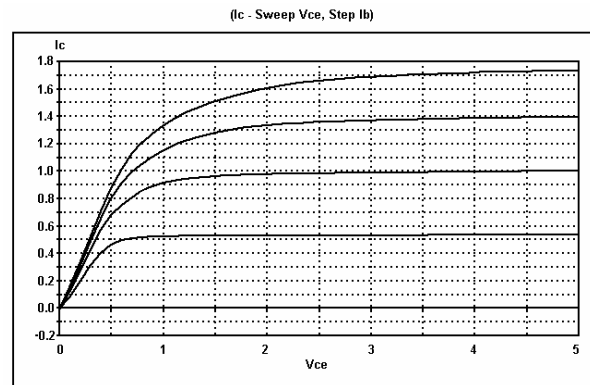


Figure 3 – Bipolar Collector Characteristics

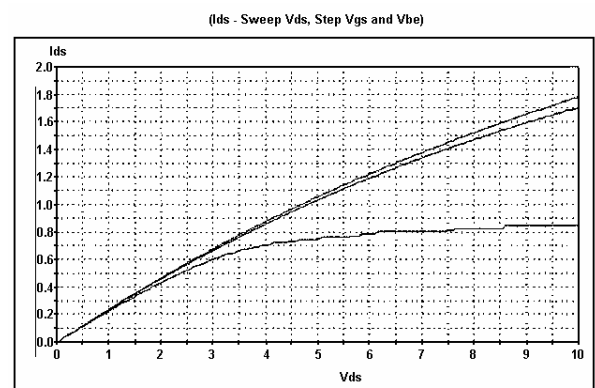


Figure 4 – Depletion MOSFET Drain Characteristics

Intradi	#	Test_Name	Units	Total	Min Exec	Max Exec	Avg Exec	Total Exec
M1	1	Igd current.v1	Volts	13,500	00:00:00.102	00:00:01.660	00:00:00.147	00:33:08.064
	2	GS BV at 500uA.v1	Volts	13,500	00:00:00.017	00:00:00.060	00:00:00.032	00:07:05.920
	3	Return result at 500uA.v1		13,500	00:00:00.000	00:00:00.000	00:00:00.000	00:00:00.341
	4	BVdsx: Is<1mA, Vds=1650 V.v1	Volts	12,304	00:00:00.096	00:00:00.229	00:00:00.146	00:29:56.911
	5	GS BV at 50uA.v1	Volts	13,500	00:00:00.018	00:00:00.046	00:00:00.021	00:04:42.197
	6	Return result at 50uA.v1		13,500	00:00:00.000	00:00:00.000	00:00:00.000	00:00:00.324
	7	BVdsx: Is<100uA, LotTestTimeReport;1.Test_Name (String)			00:00:00.092	00:00:00.194	00:00:00.111	00:22:11.348
	8	Rds(On).v1	Ohms	13,500	00:00:00.019	00:00:00.046	00:00:00.020	00:04:30.057
	9	Id(ON).v1	Amps	13,500	00:00:00.020	00:00:00.021	00:00:00.020	00:04:34.943
	10	Ids at Vgs=-3 V, Vds=2 V.v1	Amps	13,500	00:00:00.021	00:00:00.023	00:00:00.022	00:06:00.402
	11	Ids at Vgs=-8 V, Vds=2 V.v1	Amps	13,500	00:00:00.018	00:00:00.020	00:00:00.019	00:04:18.246
	12	Ids at Vgs=-10 V, Vds=2 V.v1	Amps	13,500	00:00:00.017	00:00:00.046	00:00:00.018	00:04:05.063
	13	Igl current.v1	Amps	13,500	00:00:00.017	00:00:00.044	00:00:00.018	00:03:59.278
	14	Vth @ Vds=10 V, Id=100uA.v1	Volts	13,500	00:00:00.041	00:00:01.238	00:00:00.046	00:10:14.582
	15	Vth @ Vds=1 V, Id=100 uA.v1	Volts	13,500	00:00:00.045	00:00:01.241	00:00:00.048	00:10:51.877
	16	Delta Vth.v1	Volts	13,500	00:00:00.000	00:00:00.028	00:00:00.000	00:00:03.004
Total Test Time:								02:24:42.630

Figure 5 - Test Time Report from Acquire

Setting Up Test Plans with Build

RDS Intranet features described in the preceding pages are accessed through the Build application. The test list edit screen shown in figure 6 is used to specify tests to run per intradie or module. New and existing tests can be inserted, cut, copied, etc. Tests to be skipped upon test passing or failing can also be set.

One of more tests can be executed within Build to look for interaction issues between tests/structures. If the checkbox next to test is filled, that test will be executed during automatic probing. This allows for leaving non-production, characterization tests in a test list.

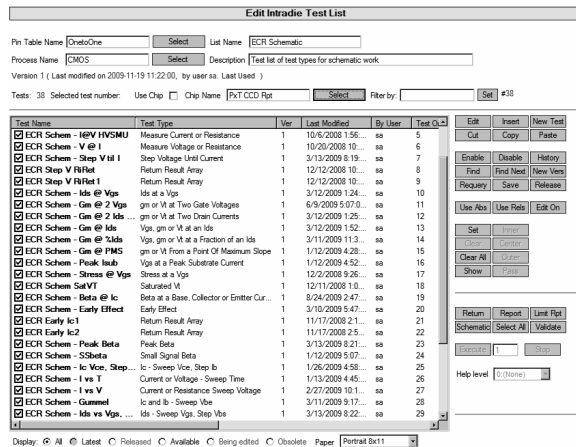


Figure 6 – Build Test List Editor

Setting Up Die Patterns

Graphical die pattern editor is used to quickly create probe patterns, including the 9 site pattern one shown in figure 8. Other die pattern editor features include:

- Up to four different test patterns can be run
- Separate die move and prober alignment sizes
- Single die X & Y offset step for misplaced PCMs
- Separate target and first die locations
- Tool to select all die and remove outliers

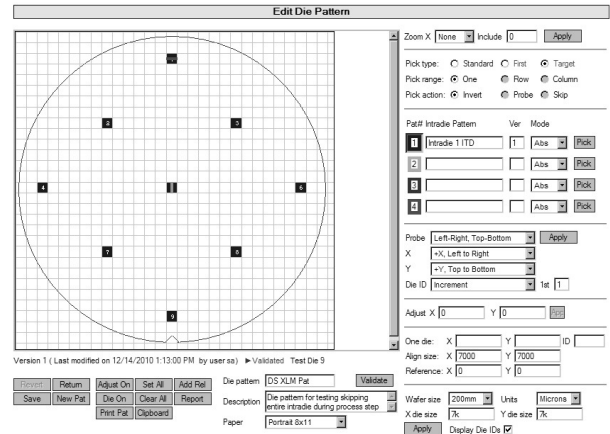


Figure 8 – Build Die Pattern Editor

Pattern Creation for Intradie Probing

Shown in Figure 7 is the graphical module editor, which gives a visual image of what is being probed. Each location can be dragged into position or its position can be entered using X and Y coordinates. A graphical editor for scribe line probing and a spreadsheet editor are also available. A test list would be created and assigned to each intradie location in figure 7.

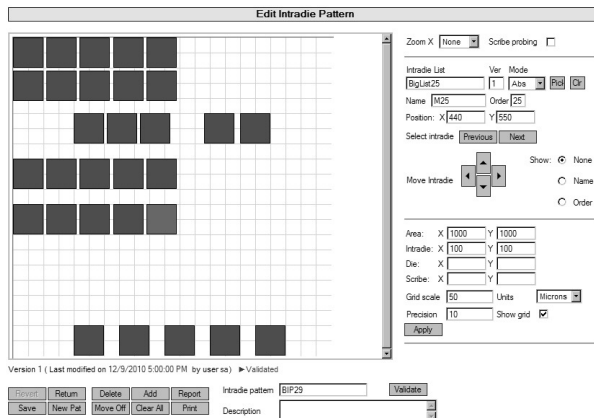


Figure 7 – Build Intradie Pattern Editor

Prober Control

RDS Intranet prober control is a good example of the flexible architecture used throughout the application. Wafer angle is separate from the die pattern and module site layout, with probe patterns automatically rotated based upon the selected angle. This allows the same pattern to be used on different probers without editing die patterns—which can be an issue when a new prober is introduced that uses a different probe card orientation. Other selections in setting up the prober are shown in figure 9.

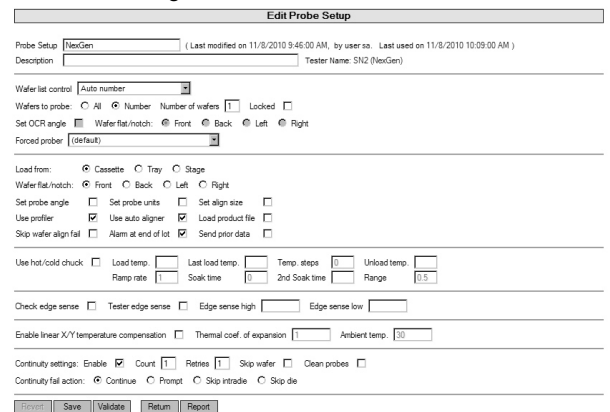


Figure 9 – Build Prober Setup Screen

Executing Test Plans with Acquire

Acquire is used for automated testing of recipes created in Build. These screens and the previous ones do not do the application justice. The true breadth of RDS Intranet is best understood with a demonstration, either on-line or at Reedholm.

Operator Interface

Figure 10 is an example input screen that an operator would populate prior to starting a lot. Almost all of the data could be imported from a workflow system tracking wafer lots.

Figure 10 – Acquire Wafer Lot Start Screen

Run-Time Test Data

The run-time screen, figure 11, displays critical probe status such as current wafer, site being tested, status of wafers already tested, etc. Individual test results can also be seen on the fly, including pausing after each intradie is tested.

Die	Die Order	Intradie	Intradie Order	Test Name	Test Order	Result	Status	Fail Code	State
1	1	M1	2	Fixed value 118.195	1	118.195	0	0	255
1	1	M1	2	Fixed value 133.288	2	133.288	0	0	255
1	1	M1	2	Fixed value 159.607	3	159.607	0	0	255
1	1	M1	2	Fixed value 175.654	4	175.654	0	0	255
1	1	M1	2	Fixed value 191.593	5	191.593	0	0	255
1	1	M1	2	Fixed value 208.123	6	208.123	3	0	255
1	1	M1	2	TLM -r (con coeff)	7	0.986444	0	0	255
1	1	M1	2	Lt	8	13.9814	0	0	255
1	1	M1	2	Rp	9	305.62	0	0	255
1	1	M1	2	Rc	10	4.27301	0	0	255
1	1	M1	2	Rap	11	0.000597428	0	0	255
1	1	M1	2	Slope	12	3.66013	0	0	255
1	1	M1	2	Y Int	13	102.348	0	0	255

Figure 11 – Build Intradie Pattern Editor

Advantages of an SQL Database

Employing an SQL database for both test recipes and results has numerous advantages:

- Rapid changes to dozens of tests can be made with simple SQL queries.
- Single tests, die patterns, limit tables, etc. can be shared using database keys so that a change only has to be made once to effect dozens of products (figure 12).
- External SQL queries can be written to perform data mining for yield improvements.
- Other tools can insert new product data and die pattern when a new mask is released.
- Workflow systems can populate tables that identify which lots and wafers are to be tested, along with the test recipes.

With the Enterprise Edition, control of the separate RDS server is usually assumed by IT, relieving the yield group from application and database maintenance, backups, etc. All that is needed on the test floor is a Windows PC with a browser and two NIC's per system.

Incorporating RDS Intranet into a workflow system is usually done with SQL scripts. And since most IT groups are flush with SQL resources, the yield team can also leverage IT for that work. The following Acquire hooks are similar to the Agilent SPECS® calls for integration into factory workflow software.

- UserLotStart, UserLotEnd
- UserWaferStart, UserWaferEnd
- UserWaferParseStart, UserWaferParseEnd
- UserDieStart, UserDieEnd

Data Storage and Extraction

During training, the engineer tasked with bringing the RDS Intranet on-line is shown how to input test data, investigate and optimize results, and control the prober. What he or she does not have to do is figure out what to do with test data. That is, decide:

- Where to store and what format to use?
- How to provide access?

These questions are moot because all data is in the database accessed directly or with Reedholm reporting and analysis tools, such as the wafer map in figure 13.

Exporting Data

In addition, data can be automatically exported in CSV (flat ASCII) and XML file formats compatible with most spreadsheets, databases, and analysis packages.

Many Reedholm customers use Excel® to augment the Microsoft Reports package provided with each system and that Reedholm used to generate standard lot and wafer reports.

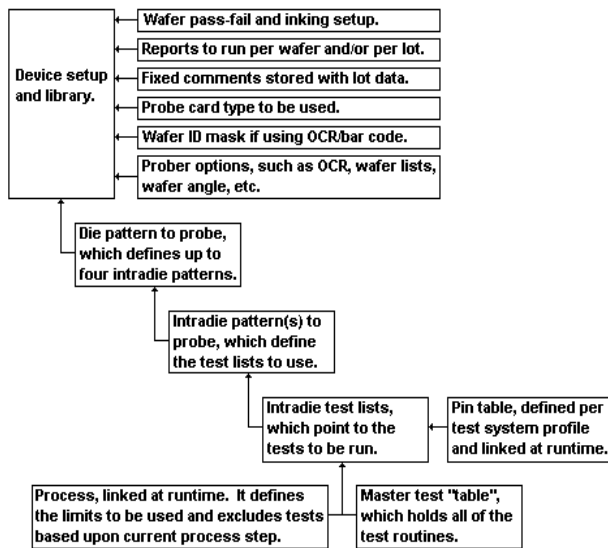


Figure 12 – Database Recipe Hierarchy

Analyzing Data with Examine

Even though most operations have existing tools to analyze the volume of data generated by a dc parametric system, RDS Intranet comes with a set of tools for smaller companies and instant, easy data crunching:

- Twenty-four reports are provided for raw data, summary data (std dev, min/max, etc.), wafer pass/fail, average time per test, and so on.
- X-Y plot tool for characterization data that includes tangents, overlaying data, applying equations, scaling, labeling, and saving to JPEG.
- Wafer map tool: 3-D, gradient, surface, exact value, pass/pail, binned, etc.
- Statistical tools that generate histograms, scatter plots, normal plots, and trend charts.

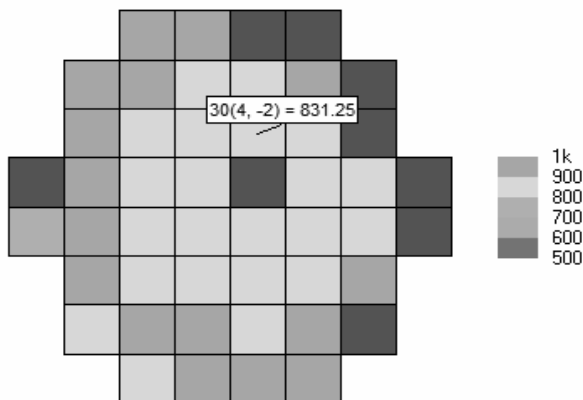


Figure 13 - Examine Wafer Map

System Administration

RDS Intranet comes with a set of software tools used to maintain the system and database, plus monitor system wide activity:

- SelfCal program keeps system in calibration.
- Diagnostics confirms system out to probe card.
- DB maintenance tool checks and repairs database tables for problems and performance.
- Activity tool lets administrator monitor active users and systems from desktop.
- Tool for confirming prober communication, which is common task after prober PM is done.

Keeping Current & Test Plan Migration

RDS Intranet software is continuously upgraded, enabling test systems to remain in service for decades. Automated migration paths for test plans make it possible to upgrade software or install improved or additional instrumentation without downtime. And migration is not limited to RDS Intranet. For instance, RDS DOS test plans can be automatically imported into RDS Intranet.

Comprehensive Training and Support

The goal of Reedholm training is to have new users ready to populate test plans and set up probing patterns. While training can be done on-site for a surcharge, doing it at Reedholm minimizes interruptions and maximizes learning. User training covers:

- Building test plans and probe patterns
- Device characterization and test optimization
- Data analysis and database maintenance
- Basic system maintenance
- Importing DOS test plans if upgrading

If part of an upgrade from RDS DOS, extra days are allotted to assist in importing RDS DOS test plans.

Online Help

On-line user manuals describe instrumentation and application software operation down to the bit level. The help system is indexed and searchable.

Real-Time Hands-on Assistance

Applications assistance is provided via the Internet using GoToMyPC software. With it, Reedholm engineers can control a system anywhere in the world to:

- Run maintenance programs.
- Troubleshoot device test issues.
- Apply software patches.

In addition, telephone, fax, and e-mail support is available from the U.S. Monday through Friday, excluding holidays. Local technical support from Reedholm distributors is also available in many parts of the world.

RDS Intranet Deliverables

RDS Intranet has three computing elements:

- Host for SQL Server and RDS application
- Windows-based test client for system operation
- DOS-based computer for real-time test control

The simplest implementation is called the Lab Edition. It combines database hosting with the test client function. This implementation is aimed at small test functions. If several users need access to the stored data, or if there are multiple instrument sets, the test client and database hosting functions are separated in what is called the Enterprise Edition. Figure 14 is an Enterprise configuration with a single set of test instruments. Each set of test instruments has a test controller for instrument and prober control. More instrument sets and test clients are added as demand increases.

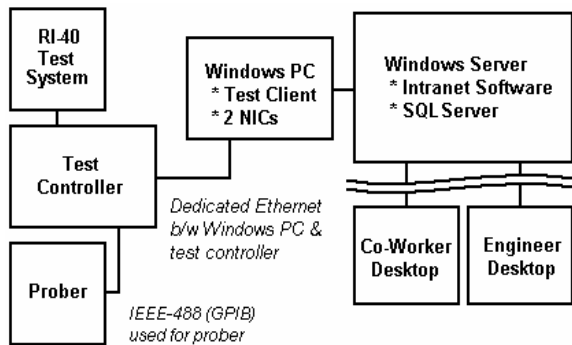


Figure 14 – RDS Intranet Computer Layout

Enterprise Edition Deliverables

- Multicore server w/ RAID 5 disk subsystem
- Windows 2003 Server OS (2008 not supported)
- SQL Server Standard w/ MS Reports
- Windows XP PC per system (7 not supported)
- Small network switch for server to client hookup

Lab Edition Deliverables

- Multicore PC w/ RAID 1 disk subsystem
- Windows XP OS (7 not supported)
- SQL Server Workgroup w/ MS Reports

Common Deliverable

- External USB HD for database backups
- CAT5 cabling for connecting computers
- KVM and cabling for each PC/controller pair

RDS Intranet Options

Software for each test controller is licensed for access to all standard features including one prober driver. Non-standard options are purchased separately and include:

- Support of specific 3rd party instruments
- Integrated thermal chuck control (ITCC)
- WLR, TCR, & CCD test routines
- Additional prober drivers