APPLICATION NOTE

JFET Gate Current Measurements

I) Introduction

A customer with a picoammeter matrix (PAM) card and a low leakage probe card, both from Reedholm, had a new requirement to measure gate current of junction field effect transistors (JFET's), but was unsure that it could be done rapidly enough for in-line testing. The evaluation performed by Reedholm showed that sub-pA gate leakage testing could be done in <1 second per die, and faster if there was no leakage introduced by device packaging or the probe card. At 200msec test times, uncertainties could be <±100fA.

These conclusions were based on gate leakage current measurements of four JFET's bonded in TO-5 type cans. They were tested at Reedholm on a PAM based RI-40 with a PCIA interface and a low leakage DUT card. The quality of the test fixturing was more than adequate for measuring the true current leakage of the JFET's. Data was also generated for an open socket condition and for a Motorola 2N5486 JFET.

II) Experiment Setup

Figure 1 shows one of the TO-5 packaged JFET's plugged into a low leakage DUT socket attached to a blank PCIA low leakage card. The Probe Card Interface Assembly (PCIA) is a low noise, shielded interface designed to drop into the opening for a standard rectangular probe card ring adapter. In laying out the DUT card, care was taken to keep any of the sixteen wires from touching one another, the DUT socket, or the board except where the wires were soldered. As a result, leakage current was almost as good as that of a blank PCIA card. After cleaning the socket with virgin isopropyl alcohol, leakage current was determined to be entirely due to the residual surface and bulk resistivity of the diallyl phthalate DUT socket.

EMAGE (test software with curve tracing features) was used to characterize system and device performance. The small amount of line frequency related noise was not a factor in making good measurements. All data shown in table 1 was taken with EMPAC.

III) Testing Considerations

The testing issue is about measuring JFET's, not the basic capabilities of a Reedholm test system. However, as a baseline, settling time to a current measurement uncertainty of ±100fA with a 15V bias was shown to be around 100msec. No averaging was required to deal with a.c. noise pick-up without the DUT card. Adding a DUT card results in more a.c. line pick-up, and adding a DUT socket results in leakage currents that a probe card would not have. As can be seen in table 1, the DUT card used in this evaluation added enough noise and dielectric absorption that it took around one second to achieve measurements with a span of ±50fA.

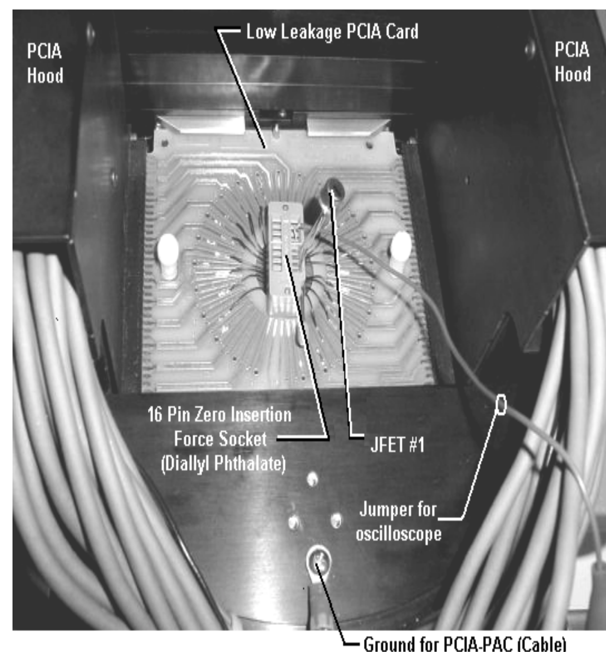

Figure 1- PCIA and DUT Card

A) Alleviating Noise Effects

Much of the a.c. line pick-up is eliminated through use of an integrating A/D converter. However, the integration is not perfect, so very large a.c. pick-up produces a signal that is too large to be eliminated by the A/D. Since the gate of the JFET's was tied to the TO-5 can, and since current was being measured on the gate, a.c. pick-up was enhanced compared to what it would be with a probe card. In order to bring the digitized peak-to-peak noise down to ±100fA, four readings had to be averaged.

B) Settling Time

At low currents, the time decay of current within insulators due to voltage steps must be considered. For times beyond a few milliseconds, this decay is largely polarization current, or dielectric absorption (DA).

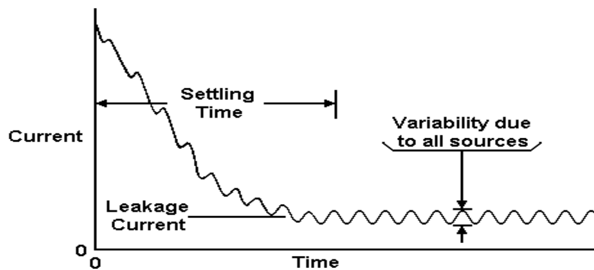

Figure 2 - Noise & Settling Time Issues

Design of the Reedholm PAM's and low leakage cards virtually eliminates DA compared to the amount of DA found in items such as the diallyl phthalate socket on the DUT card. Furthermore, the JFET packaging had more DA than the socket on the DUT card.

Regardless of the reasons for why it takes longer than expected for current to reach its final value, starting to take data before the current has finished changing will produce inaccurate results.

Figure 2 is an illustration of the visualization that has to be used in setting up test parameters. That is, one has to make sure that the final measurement is not started before the end of the settling time even if one has to use averaging techniques to remove the signal variability.

1) Use of Auto-Ranging for Delay

If auto-ranging techniques are used, and if one knows that several range changes are going to occur before the final reading is taken (as is the case for currents <90pA), the time required for each range decision can be used to make sure that the minimum settling time has occurred.

Since auto-ranging was used for this evaluation, a very short (10msec) initial EMPAC delay could be used without affecting accuracy.

C) Problems with PAM Overload

While no damage results to the DUT or PAM due to charge coupling, low current measurements are often compromised by charge coupling through the DUT. Figure 3 is a simplified schematic of the front end of the Reedholm PAM (along with the DUT and the bias source). Other low current instruments, including electrometers, are similarly configured. Feedback resistors have to be very high value to convert small currents to reasonable voltage levels, and feedback capacitors have to be small as possible to minimize test times. For example, the 5pF capacitor and the 1GΩ resistor in figure 3 for the 100pA and 1nA ranges produce a time constant of five milliseconds. That is quite slow given the bandwidth of the op amp being used.

1) Amplifier Saturation

Since the amplifier uses ±15V supplies, any input signal that forces the amplifier output to within a volt or two of the 15V supplies causes saturation in the amplifier and produces a relatively long recovery time (several seconds) after saturation. In order to have short test times when measuring low currents, one needs to make sure that test conditions do not cause the PAM amplifier to saturate. That takes some care, and is not simply a matter of minimizing the current being measured—charge coupling must be considered.

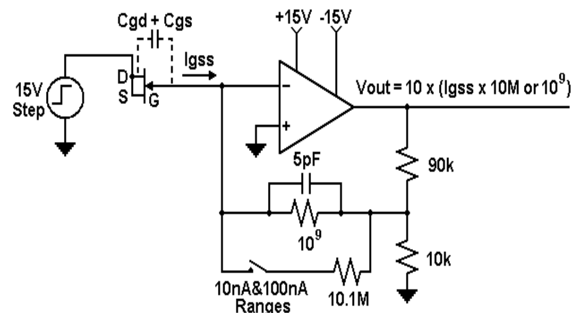

Figure 3 - Simplified Test Schematic

2) Charge Coupling from DUT

On the most sensitive range, gate-to-drain and gate-to-source capacitances couple the 15V test signal edge directly to the amplifier. The only thing that keeps the amplifier from saturating is the 5pF feedback capacitor. As the feedback string provides a gain of 10, and as the amplifier output is limited to 15V, saturation happens when the combined gate capacitance (Cgs + Cgd) approaches 0.5pF.

3) Additional Charge Coupling

On the practical side, there is capacitive coupling from the DUT card and matrix to the gate pin as well as from the gate capacitance. Thus, the gate capacitance budget needs to be much lower than 0.5pF. In the open socket condition, overload did not happen on the most sensitive (100pA) range, but the large impulse resulting from the 15V test signal step implied a fringing capacitance of 0.3pF.

4) Preventing Overload

These three methods are useful in preventing overload of the PAM.

- Use smaller steps in reaching the 15V test level. Each step has to have enough delay to allow the 5pF capacitor to discharge before the next step.
- Use a much lower current for current limiting (<6nA) so that the maximum coupling current is kept <1nA. This works because the current used for the power supply must charge the system capacitance of around 300pF.
- Start measurements on a higher range and permit auto-ranging down to the lowest current range. As one can see in figure 3, the 10nA and 100nA ranges use a 10MΩ instead of a 1GΩ feedback resistor. As a result, the amplifier never saturated (for the case of this evaluation).

IV) Test Method

A) Start on the 100nA Range

For this evaluation, the auto-ranging scheme was used to eliminate PAM saturation. Data was taken starting on the 100nA range, but the 10nA range would have worked as well. Doing so would have produced test times approximately 200 milliseconds faster than shown in table 1.

B) Range of Devices Tested

A summary of the test results is shown in table 1. As there were some problems achieving the wafer level gate leakage currents taken by the customer using a bench electrometer and individual micro-probes, data was also taken open socket and with a plastic packaged Motorola 2N5486 JFET. A 10MΩ oscilloscope probe was connected directly to the drain to monitor test and timing conditions.

C) Timing Results and Test Conditions

EMPAC is a test plan creation and editing package that permits timing of individual tests through use of the <Alt> <F2> function key combination. In addition to calculating test times, the <Alt> <F2> combination generates average, minimum, maximum, and standard deviation when a test is put into a looping mode. All four data types are provided in the first four rows of table 1. The tests that generated the data took an average of 1.1 seconds under these conditions:

- Drain, source, and oscilloscope pins were shorted together and biased at 15V.
- There was an initial 10msec delay before averaging four readings using the PAM.
- Autoranging started on the 100nA range.
- Loops of five tests were run.

The fifth row in table 1 shows the asymptotic current that is reached with very long test times (17sec). Since the open socket current is effectively zero, the other results are true leakage currents.

Test Time (seconds)	Data Type	Open DUT Socket	2N5486	DUT 1		DUT 2	DUT 3	DUT 4
				Initial	Cleaned			
1.1	Average	32.5	508	1100	665	895	3300	3080
	Minimum	0	438	763	550	763	2850	2713
	Maximum	100	613	1738	913	1200	4088	3838
	Std Dev.	40	69	396	145	178	499	449
17.0	Average	13	363	N/A	363	525	1988	1925

Table 1 - Measured Currents in femto-amperes

D) Initial Results Before Cleaning DUT #1

During initial testing, it appeared that DUT#1 had quite a bit of gate leakage. On the first day, the current was around 2.5pA after 1.1 seconds and seemed to asymptote to 1.34pA after 17 seconds. In addition, there was a lot of variability. However, the open DUT socket measurements and those on the 2N5486 did not exhibit that variability or level of leakage.

E) Results After Cleaning

On the next day, it was less humid outside, and the leakage current was lower as shown in table 1 labeled "initial". Since the symptoms are similar to what is seen at Reedholm when probe cards are not adequately cleaned, it was postulated that the problem was contamination on the glass surface of the TO-5 can. Virgin isopropyl alcohol and cotton swabs were used to clean DUT#1 followed by baking it for 15 minutes at 50ºC. The much lower results after cooling down are shown in the column labeled "Cleaned". No attempt was made to clean the other JFET's, but it appears that DUT#3 and #4 could have used it.

Since the gate leakage for the plastic packaged 2N5486 has much less variability, it probably has much less contamination due to packaging than the TO-5 JFET's. Nevertheless, it could be that the 2N5486 packaging is responsible for the leakage current actually measured. The 2N5486 was not cleaned.

V) Projections for Wafer Testing

Undiced JFET's are not contaminated by packaging, and well processed JFET leakage currents approach 0fA. In such cases, test times could be more aggressive since the test limit budget would not have to include any JFET leakage. That is, with true junction leakage close to zero, one only has to wait long enough for systematic current to fall below 1pA. With Reedholm low current cards, that can take as little as 100msec. On the other hand, if leakage approaches 1pA, one needs to wait longer to keep from rejecting adequate devices.

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