APPLICATION NOTE

BV_{CEO} Breakdown Measurements

Overview

Measuring BV_{CEO} is tricky at any voltage, and is a slow test at low I_C because any charge injected into the base when biasing the transistor has to fully recombine before an accurate measurement can be made. Several Reedholm routines used to directly find BV_{CEO} are characterized in terms of speed and resolution, illustrating the speed issue. In addition, a couple of methods are described that produce results much faster than the direct method of measuring BV_{CEO} at a specific I_C.

Some information on BV_{CBO} and BV_{CES} testing gathered while preparing this note is included. Other information on bipolar transistor breakdown is in support note AN-122, Breakdown Voltage Tests Including Bipolar Transistors.

Types of Bipolar Breakdown

Three types of bipolar breakdown shown in figure 1 are based on illustrations in bipolar transistor test books. It is straightforward to generate BV_{CBO} plots, but the other two are tougher because current gain at very low charge injection from the collector-base re- gion leads rapidly to operation in the lower voltage regions.

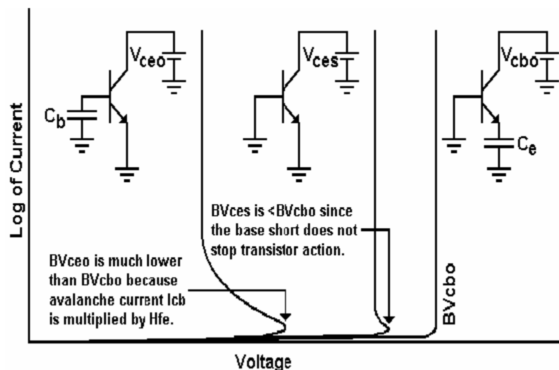

Figure 1 – Types of Bipolar Collector Breakdown

After the knee, BV_{CBO} has a slight positive slope due to base and collector region resistance. The slope of BV_{CEO} after the foldback is complicated by the dependence of BV_{CEO} on current gain and BV_{CBO}.

BV_{CEO} Using Force I, Measure V

The fastest direct method for measuring BV_{CEO}, i.e., with the base open, is to force current and measure the resultant voltage.

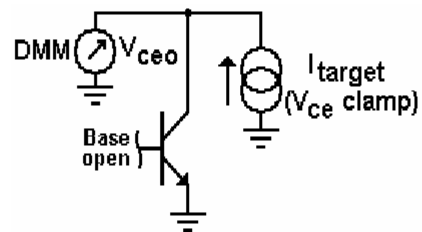

Figure 2 - BV_{CEO} at $I_B = 0$

At higher currents, direct measurements are not too slow, but making measurements with the base open and with excessive resolution requirements results in very slow tests. The sweep in figure 3 shows how long it can take in seconds for charge injected into the base to recombine and thus for V_{CE} to reach equilibrium.

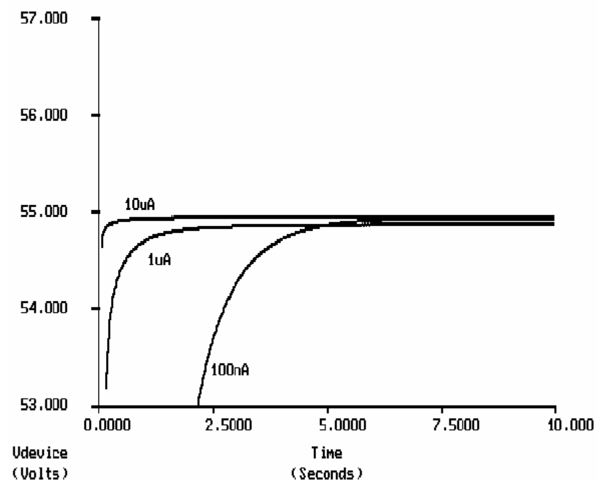

Figure 3 - Time Required for BV_{CEO} to Stabilize

These types of delays are not highly dependent on the test system. Users of directly connected digital curve tracers incur similar delays if there is any con- nection to the base.

Although the plots in figure 3 indicate times that are not realistic for automatic testing, sometimes there are requests to measure BV_{CEO} at lower currents. Figure 4 illustrates 10nA response as well as providing a closer look at the 100nA response of figure 3.

Overshoot at Very Low Currents

When swept for much longer times than seem necessary, there is an interesting phenomenon at lower currents. The overshoot after reaching and exceeding a quiescent level is shown on the right axis. Excess base charge with long recovery must be responsible for the overshoot. The phenomenon appears similar to de-trapping during tunnel oxide stressing.

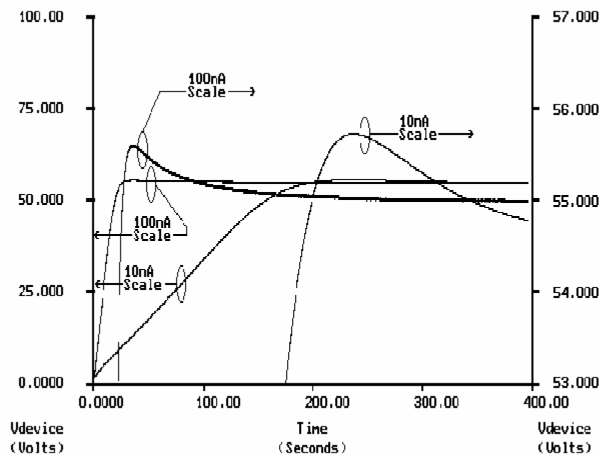

Figure 4 - VCEO Response at 10nA & 100nA

BV_{CEO} Force I, Measure V Test Times

Since response times at lower currents would be too long for practical use in automatic testing, the data in table 1 was taken for currents from 1µA to 100µA. Times are in msec and voltages in volts.

- The longest times use delays to assure the final value, but were not arbitrarily long. Any shorter and the final value was not reached.
- The second row contains times and voltages to nominally be within 1% of final values.
- The bottom row has results to nominally be within 5% of final values

1µA		10µA		100µA	
Time	**V_{CE}**	**Time**	**V_{CE}**	**Time**	**V_{CE}**
4662	54.7	836	54.5	102	54.8
3163	53.8	436	54.0	32	54.1
2166	51.5	136	51.3	29	51.4

Table 1 - V at I Test Times for BV_{CEO}

BV_{CEO} Using Stepped Voltage

Until the force current, measure voltage routines were changed to make it easier to capture voltages prior to breakdown, some customers used a stepped voltage test to make bipolar breakdown measurements. However, the stepped voltage method is considerably slower than forcing current.

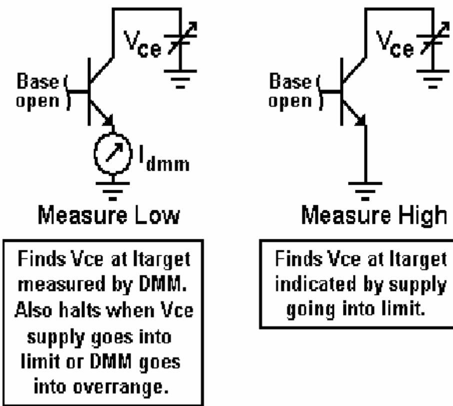

Figure 5 - Stepped BV_{CEO} Methods

Measure in Low Leg

Table 2 shows results with two target voltages, 1% less than the final value and 5% lower. Getting spe- cific values with a stepped routine is difficult, but these results are representative.

These tests were so time consuming that results were checked a couple of times. Autoranging was not a factor. Fix range measurements were made on one range higher than targeted. Compliance current on the stepping supply was set to one range higher. Delays were minimized for each step size.

Step Size (mV)	Target Voltage			
	BV_{CEO} – 1%		BV_{CEO} – 5%	
	Time (msec)	Final V_{CE} (V)	Time (msec)	Final V_{CE} (V)
500	7747	54.0	3247	51.6
200	11085		3602	51.5
100	13488		4713	51.7

Table 2 - Stepped BV_{CEO} to I_E = 1µA Using DMM

Times were much lower at higher currents, but still so long that another table was not created. With 500mV steps, it took:

- 565msec to reach 54.0V at 10µA
- 135msec to reach 54.5V at 100µA

Measure in High Leg

Measuring in the high leg means using the limit bit in the stepping supply to flag being in or out of limit. This mode is slower than using the DMM as can be seen in Table 2 shows results with two target voltages, 1% less than the final value and 5% lower. Getting specific values with a stepped routine is difficult, but these results are representative. They were so time consuming that results were checked a couple of times.

Step Size (mV)	Target Voltage			
	BV_{CEO} – 1%		BV_{CEO} – 5%	
	Time (msec)	Final V_{CE} (V)	Time (msec)	Final V_{CE} (V)
500	12082	54.0	4776	51.5
200	15110		5365	51.6
100	16565		5551	51.7

Table 3 - Stepped BV_{CEO} to I_E = 1µA Using Limit Bit

Stepped Voltage Response Time Analysis

Transforming a voltage versus time sweep and overlaying it on a current versus voltage sweep generated the plot in figure 6. The left axis shows how steep the current response is and the voltage. The curve on the right shows how long it takes to reach the final voltage at 50nA. Notice that the voltage at 50nA is essentially the same as voltage at 562µA.

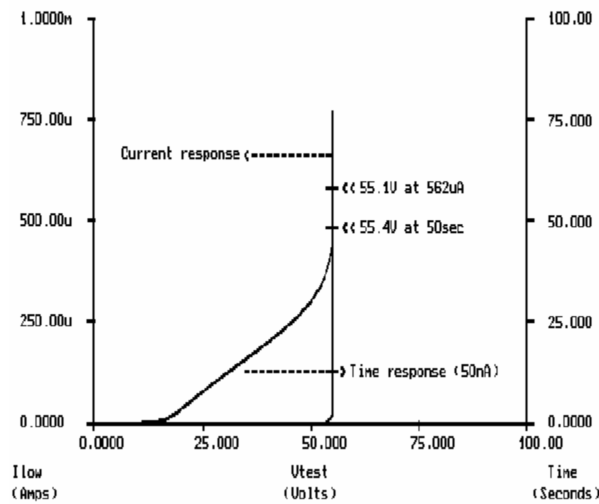

Figure 6 - Current & Time Versus Voltage

BV_{CEO} From I_B Zero Crossing

Test times from direct measurements of BV_{CEO} are so slow that it is hard to understand how users could make them process control tests. More than likely, delays are arbitrarily shortened to meet production test time requirements. If so, their accuracy is as suspect as inter-layer current leakage measurements that only measure test system characteristics, and not those of a device.

Fortunately, a significantly faster method is to force current in or out of the emitter and step collector voltage until the base current goes through zero current (figure 6). This method has been used for many years with digital curve tracers to quickly get a reliable, repeatable value.

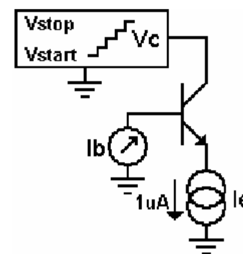

Figure 7- BV_{CEO} at I_B = 0

Figure 7 shows I_B as V_{CB} was increased in 100mV steps through BV_{CEO} with I_E = 1µA. Forcing I_E instead of I_C has no practical effect on BV_{CEO} value because avalanche breakdown current increases by orders of magnitude within a few mV of initiating breakdown.

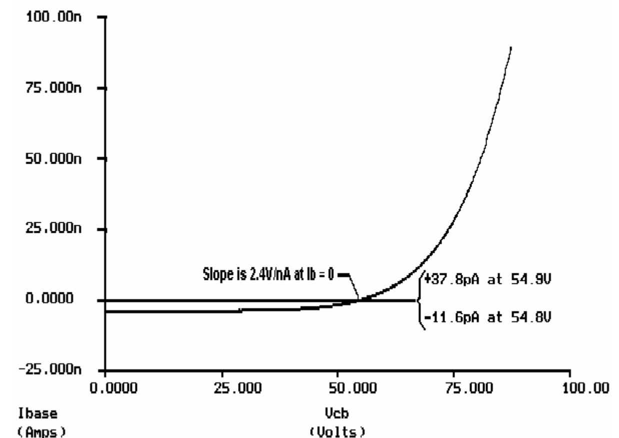

Figure 8 - I_B with Stepped V_C

A prior test measuring V_{BE} at I_E of 1µA produced 486mV. That voltage needs to be added to the final V_{CB} in table X to produce BV_{CEO}.

Step Size (mV)	Starting Voltage			
	0V		25V	
	Time (msec)	Final V_{CB} (V)	Time (msec)	Final V_{CB} (V)
500	265	53.5	161	54.0
200	604	54.0	336	53.4
100	1169	53.8	645	53.9

Table 4 - Stepped BV_{CEO} to I_B = 0

Test Times and Starting Voltage

Delay after each step was set to 1msec. Using a 100mV step resulted in 538 steps to get to 53.8V, and elapsed time was 1169msec, so average time per step is only 2.17msec. Of course, that average includes test overhead. Using algebra, time per step can be shown to be 2.1msec, and overhead is 40msec largely due to the charging rate calculated for the 1µA test current.

With a 1% accuracy target, step size can be as large as 500mV, and test time was 265msec. Smaller steps provide increased resolution, but at doubtful utility. Measurement error of 1% should be tolerable, even if it tends to be systematically low.

Since test time is directly related to quantity of steps, it makes sense to start testing at the highest pos- sible voltage. Using a 25V starting voltage, the same BV_{CEO} is measured in around half the time at 161msec. No additional charging time was required in starting at 25V. In practice, there is no reason to store results that clearly indicate misprocessing, so starting voltage could be 80% of the expected breakdown of 55V, or 44V. In such a case, only 22 steps would be needed, so test times would be around 88msec.

Step Voltage Considerations

Delay times can be quite short in the stepped voltage tests, but are a function of step size. Figure 9 illustrates what can happen when there is not enough delay for each 500mV step.

The top trace is the tail end of a BV_{CEO} stepped voltage test. The bottom two traces are the DMM A/D converter inputs where 5V represents full scale current, or 1mA in this case. Each voltage step causes a displacement current impulse due to coupling capacitance that has to die out before the current is measured for the test. Note that an inadequate delay results in a BV_{CEO} that is lower than it should be.

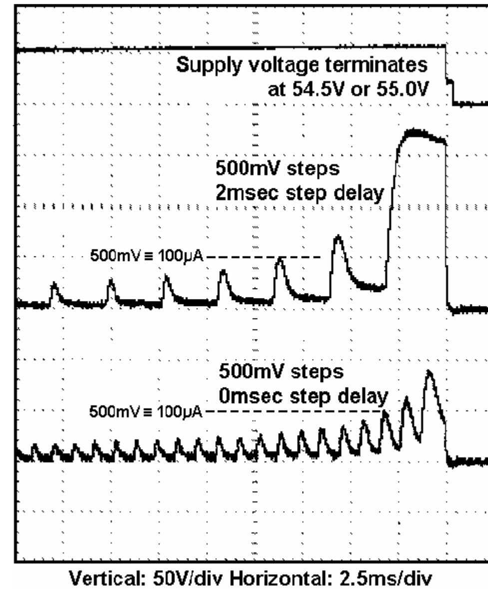

Figure 9 - Impulse Current Response to Steps

BV_{CBO} Measurements

The 200V breakdown test in figure 10 was used to find BV_{CBO} over a range of currents. Nominal voltage was 121.5V with <0.5V variation from 1µA to 100µA.

BV_{CBO} did increase by 3V at 1mA to reach 124.5V, but that increase was likely due to self-heating. That is because BV_{CBO} is the measurement of avalanche breakdown of a P-N junction. Avalanche is a very rapid process as can be seen in figure 6.

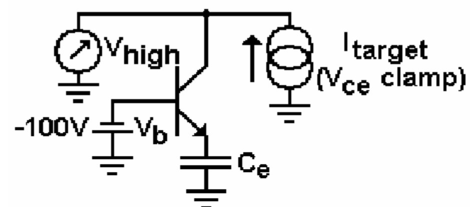

Figure 10 - BV_{CBO} Method

BV_{CEO} Using Breakdown Model

Another way to speed up testing is to use the relationship between BV_{CEO} to BV_{CBO} to make a few fast measurements and infer BV_{CEO}. Grove in Physics and Technology of Semiconductor Devices, Wiley, 1967 derives the relationship and restates the formula in Table 7.1: Important Formulas for Junction Transistors.

$$BV_{CEO} \cong \frac{BV_{CBO}}{\sqrt[n]{h_{FE}}}$$

Dependence on Current Gain

For the NPN devices Grove modeled, n was ~4. PNP devices had a root of 6. Also, h_{FE} for both types had a strong dependence on current, so it was impor- tant to extrapolate to BV at h_{FE} = 1.

Implication for Faster BV_{CEO} Results

If h_{FE} has considerable dependence on I_C, *n* can be computed from h_{FE} at a couple of currents, I_1 and I_2, as long as BV_{CEO} is measured at each current.

$$n = \frac{\ln\left(\frac{h_{FEI_1}}{h_{FEI_2}}\right)}{\ln\left(\frac{BV_{CEOI_2}}{BV_{CEOI_1}}\right)}$$

Thus, four measurements at fairly high currents could be made very quickly to determine *n*. With that value, all that is needed is h_{FE} at the desired current to

compute BV_{CEO}. Time savings can be significant since h_{FE} is a relatively quick measurement even at low cur-

rents. Using single point Acquire measurements, table 5 was populated with data from a 2N3904 transistor.

I_C	h_{FE}	Time (msec)
100µA	181.3	20
10µA	182.1	23
1µA	181.4	52
100nA	181.9	66

Table 5 – h_{FE} Measurement Times

However, current gain of the 2N3904 used for this note had little dependence on current. The sweep of h_{FE} (Beta) versus I_C in figure 11 reinforced the find- ings. A slight dip around 10µA was due to an inade- quate delay being used at a range change. Also, there is little Early effect. Changing V_{CE} from 0 to 5V only increased gain by 3%. With such little effect, current gain can be measured faster by forcing I_E, measuring I_B at a fixed V_C and not adjusting for actual V_{BE}.

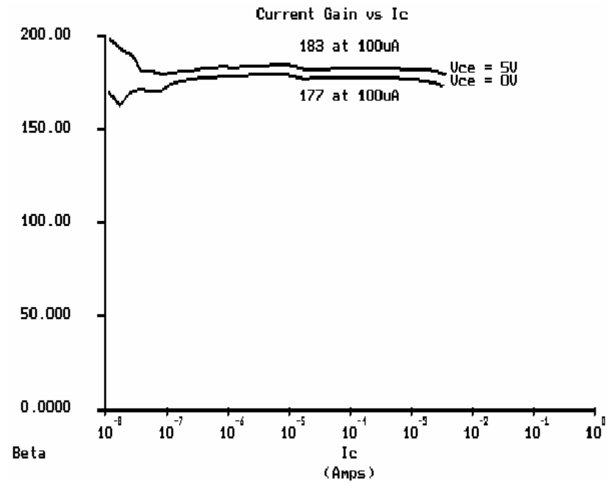

Figure 11 - 2N3904 h_{FE} versus Ic

If h_{FE} does not depend upon I_C, neither does BV_{CEO}. That was borne out in the BV_{CEO} measurements docu- mented later in this note. So, *n* could not be deter- mined from the slope of the h_{FE} versus I_C plot. Fortu- nately, the more direct approach can be used.

Extracting *n* Directly from BV_{CEO} Equation

At low currents, BV_{CEO} is slow because it takes a long time to charge/discharge parasitic and fringe capacitance with the base recombination current. But at high currents, BV_{CEO} can be measured fairly quickly as can BV_{CBO} and h_{FE}.

$$n = \frac{\ln(h_{FE})}{\ln\left(\frac{BV_{CBO}}{BV_{CEO}}\right)} = \frac{\ln(181)}{\ln\left(\frac{121.5}{55}\right)} = 6.55$$

At 100µA, BV_{CBO} was found in 40msec and BV_{CEO} in 62msec using the criteria that voltage be within 1% of final value. Since measuring h_{FE} took 20msec, finding *n* took a total of 122msec. Calculation times were in- consequential at <<1msec.

Test Time for Extracted BV_{CEO} at 1µA

Since avalanche breakdown (BV_{CBO}) is not a function of current, finding BV_{CEO} at a low current only requires one more measurement, h_{FE}.

- At 1µA, it only took 52msec to find h_{FE}, so finding BV_{CEO} took 122 + 52 = 174msec.
- Compare that with the fastest direct measurement of BV_{CEO} when forcing 1µA, which took >4 seconds to get to within 1% of the final value.
- While the time is not as fast as finding BV_{CEO} from I_B = 0, it would be much faster at lower currents or with tighter resolution.

Dealing With Sneak Paths

Previous results were from a discrete transistor. However, the three leads of bipolar transistors are seldom isolated in test structures. The rest of this note deals with the effects of sneak paths when making breakdown measurements.

The schematic in figure 12 was duplicated at Reedholm using the CA3096 test vehicle that has three NPN transistors and two PNP ones. Base, emitter, and collector of each is available plus a common substrate. To emulate the customer structure as closely as possible, the emitters of transistors 2 and 3 were connected at the IC instead of using matrix connections. Testing was done using the 200V test algorithm

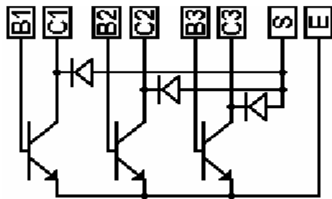

Figure 12 - Three Transistor Structure

BV_{CBO} and BV_{CES} were about the same on the CA3096 IC at 108V. That meant that the 200V test needed to be used for those measurements. BV_{EBO} was around 8V. Fortunately, this packaged device was quite rugged than the customer one that wound up with a shorted base-emitter junction when a bench curve tracer was used to measure BV_{CBO}.

Figure 13 shows the bias and connection scheme for BV_{CBO} measurements. BV_{CES} connection just ties the common emitter to the base. Of paramount consideration is that voltages applied to one transistor affect all of them. That is, as the base of one transistor moves to –100V, the common emitter is pulled to –100V + BV_{EBO}, or -92V. That causes the other two transistors to turn on because of base capacitance to ground which, in turn, pulls the substrate to –92V.

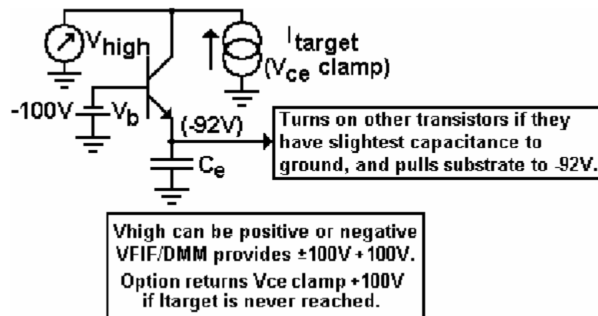

Figure 13 - Connections for BVCBO Measurements

BV_{CES} & BV_{CEO} Sneak Path Waveforms

Figure 14 shows the waveforms when the sneak paths in the structure are not connected for the BV_{CBO} test. At test power down, the base-emitter junction forward biases, causing current multiplication and relaxation oscillation during power down. In some ways that is fortunate since cycling of the transistor brings the substrate, emitter, and unused base connections to 0V before the end of the test.

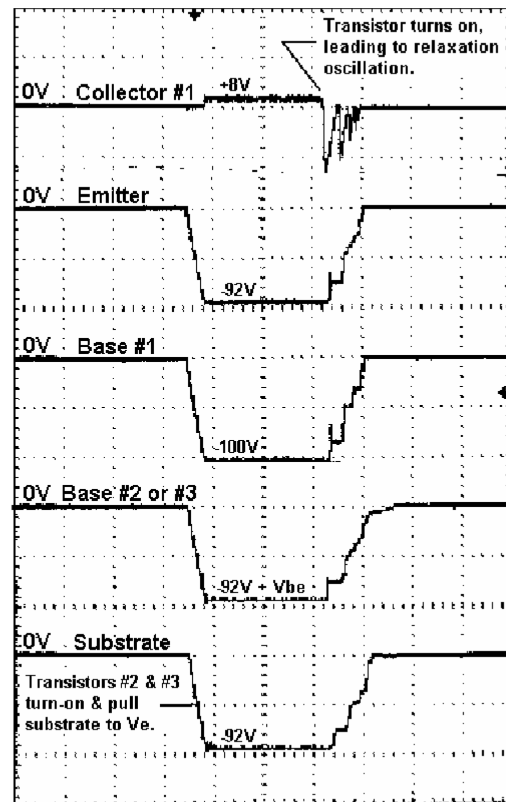

Figure 14 - BV_{CES} Waveforms

However, as shown in figure 15, there is no relaxation oscillation for the BVces test because the transistors do not turn on. The bases of transistor #2 and #3 are returned to within BV_{EBO} of ground via reverse breakdown. Furthermore, those pins are left charged at –BV_{EBO} until used on a subsequent test. Worse still, the substrate is left at around –40V until pins are grounded. Thus, a BV_{CES} test would be a likely cause of loss of instrument control and relay welding.

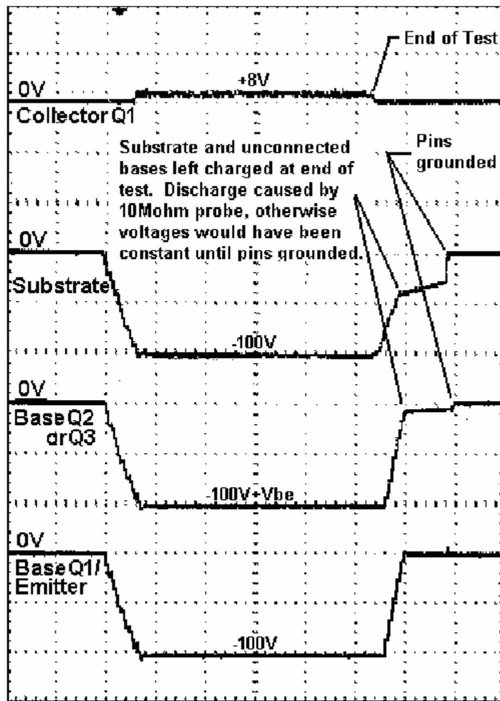

Figure 15 - BV_{CBO} Waveforms

BV_{CBO} with Sneak Paths Connected

Connecting all structure paths results in well controlled behavior and prevents hot switching. Figure 16 shows results when the unused bases are shorted to the emitter and the unused collectors and substrate tied to the base of Q1. This allowed biasing the emitter to a voltage that prevents the reverse biased collector-base region from reaching through the base to the emitter.

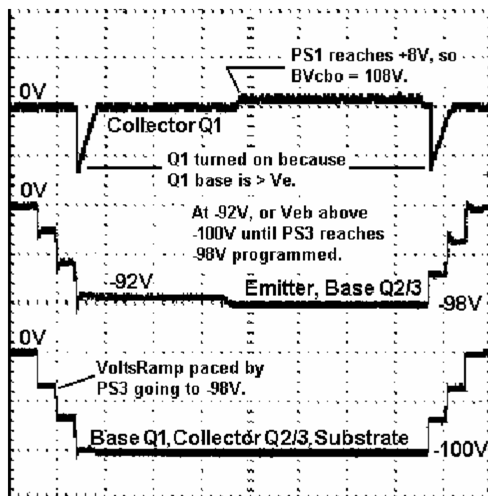

Figure 16 –BV_{CBO} with All Paths Connected

Partial Elimination Not Enough

It is not enough to connect some of the possible sneak paths and try to use test results as an indication of success. As shown in figure 17, tying unused bases to the emitter prevents transistor action by the unused transistors, but does not prevent charging through the substrate pin or through the unconnected collectors. Any residual voltage >1V should be eliminated to be sure of no hot switching.

All pins in the structure have to be connected somewhere so that the end of the test returns every pin to ground.

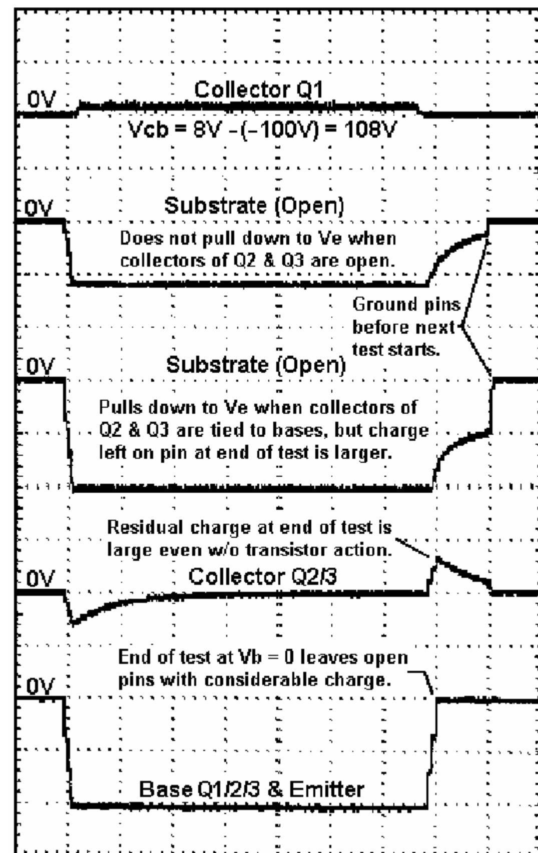

Figure 17 –Partial Connections Still Charge

Charging with HVSMU

Merely using the HVMSU does not eliminate the need to take care of sneak paths. Figure 18 shows residual charges when a stepped voltage ramp is used with the HVMSU that provides up to ±250V, thereby eliminating the need to bias the emitter to –100V.

The emitter and unconnected bases are not left with charge at the end of the test. However, there was upwards of 5V left on the unconnected collectors. Since sweep speeds were quite slow, the peak voltage may have been much higher.

Recovery Due to Scope Probe

The quick recovery from the peaks is an artifact of having a 10MΩ scope probe attached to the unconnected pins. Without the probe, the voltage at the end of the test would remain until all pins were grounded at the end of the test, and thereby incur hot switching.

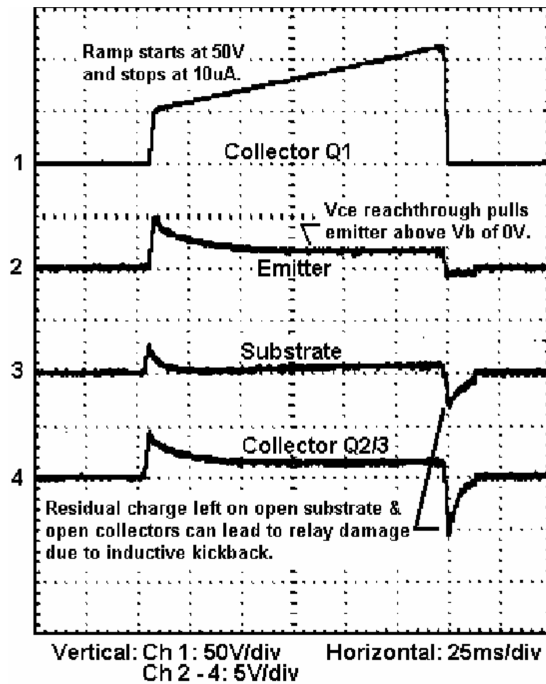

Figure 18 - Stepped BV_{CBO} Using HVSMU

Use of 200V Test at <100V

There is no restriction on breakdown voltage when using the 200V test. If BV is known to be <200V, and if sneak paths are appropriately connected, voltages <100V can be accurately measured almost as quickly as using the ±100V version.

Figure 19 is of a BVCEO test at 1µA. It is shown with a relatively fast sweep to illustrate that the waveform is well behaved. The collector waveform seems to have settled within 40msec to 46.4V, but BVCEO is really 54.5V. It would just take as long as shown in table 1 to reach the final value.

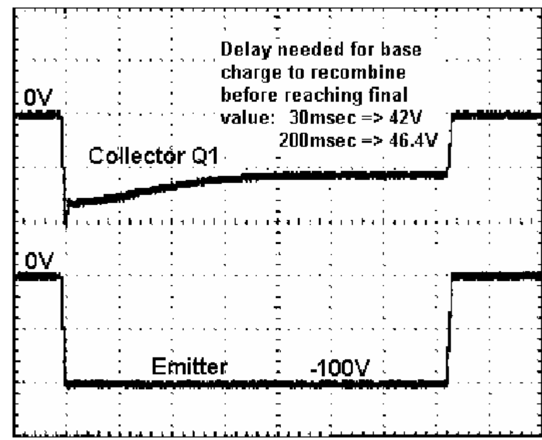

Figure 19 - BV_{CEO} at 1µA with 200V Test