REEDHOLM

DATA SHEET

DS-10055

Device Parameter Tester
Model RI-2kV/5A

- **Integrated system, not a set of boxes**
- **Testing and control without programming**
- **Fast, automated wafer testing**
- **Inexpensive, compact probing platform**
- **Rugged rectangular probe card interface**
- **No bulky and complicated test head**
- **Device parameters, not just pass/fail**
- **Backside connection to vertical devices**
- **Bipolar, FET, capacitor, & resistance**
- **Integrated device characterization**
- **2kV and 5A delivery with errors <0.05%**
- **0 to 2kV in <10msec with no overshoot**
- **Control not lost when device shorts**
- **Pulsed 5A tests: 30 to 300µsec**
- **Memory mapped instrument**
- **Microsoft SQL database**
- **Crystal Reports generated outputs**
- **CSV & XML export — Excel compatible**
- **WEB browser user interface**

High power devices built on silicon carbide and other types of substrates achieve maximum performance with vertical structures connecting the drain or collector to the wafer backside. Testing such devices on manual probers with a collection of instruments is satisfactory during early development, but low yields require reliable, high throughput testing when getting ready for market introduction.

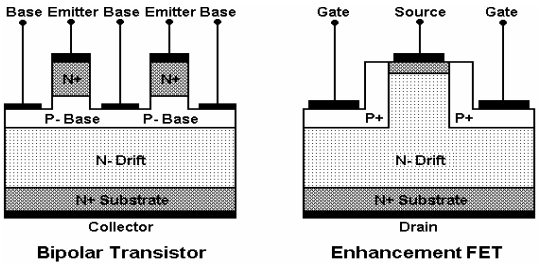


Figure 1 - Vertical Transistors

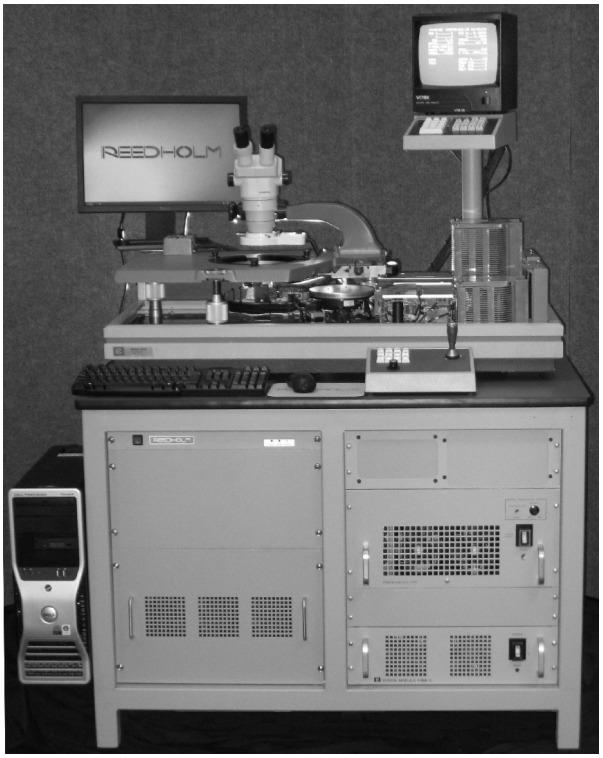


Figure 2 - Prober Platform Includes Instruments

Integrated Platform

The RI-2kV/5A is a fully integrated dc test system configured for high volume testing. Contact to the wafer backside is through Kelvin sensing leads capable of ±5A and +2kV. Instrumentation is built into the base of a low cost, high-speed prober that has been altered to be insensitive to catastrophic device breakdown. A data driven applications environment eliminates programming so that engineers responsible for the system and for interpreting its output are not diverted from device and process engineering.

A test controller mounted inside the prober table provides real-time control of instrumentation and prober. Operators and engineers access the system via a Windows computer running a test intranet application, simplifying system administration and operation.

No Instrumentation Footprint

Clean room space, whether in the fab or on the test floor, is extremely expensive. Layout dimensions in figure 3 illustrate floor space needs of the RI-2kV/5A. Some Reedholm customers move the monitor and keyboard to the prober table to save even more floor space. Competitive systems require a footprint almost as large as the prober just for the instrumentation.

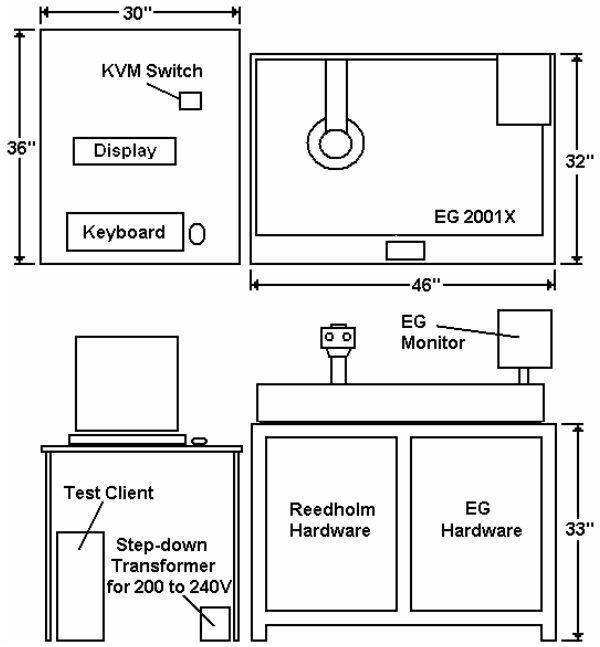


Figure 3 - Layout with Table for Monitor & Keyboard

Memory Mapped Instrument Control

The RI-2kV/5A is controlled by a single board computer (SBC) operating under a version of MS-DOS that provides real-time control and does not have latency issues associated with a multi-tasking operating system. As a result, timing measurements are accurate and repeatable down to microseconds without using an external timer counter that complicates control without addressing latency issues.

Other system architectures have processors and memories buried inside instrumentation boxes. That approach results in slower communications and lack of control of the overall system state.

With memory mapping, complex commands are transmitted at speeds much faster than achieved with IEEE-488 instrumentation buses or other serial protocols. For example, a range command is transmitted from a test plan running on the SBC to an instrument in <2µsec. As a result, the RI-2kV/5A is inherently faster than systems that depend on older UNIX® or Linux computers as well as newer multi-tasking ones.

Keeping Control at Breakdown

Proprietary prober modifications prevent rapid discharge on the chuck from locking up the prober or instrumentation. Thus, rapid decrease in device impedance at avalanche breakdown is not a problem. Nor is rapid turn-off of the supply attached to the chuck.

The cause of lock-up is rapid change in chuck voltage due to catastrophic device failure. In effect, the device is a spark generator and the chuck is the transmitter antenna. The energy pulse from destructive device breakdown generates large RF pulses that are broadcast and conducted throughout the test system. Without proper consideration, those pulses wreck havoc with prober and instrumentation memory registers.

Keeping Control with Memory Mapping

In addition to providing higher speed and tighter timing control, memory mapping means that the CPU can read and respond to the entire system state in less time than it takes for a reed relay to change state. This flat control architecture is vitally important in coping with noise generated by device breakdown.

The memory map in figure 4 is generated by a software maintenance utility that enables bit level examination and control of every instrument register using the same routines that provide uncompromised control over state of the system.

By continuously monitoring the memory map, an unintended change in any register is a flag that destructive breakdown has occurred. Because communications are so fast, all registers, and especially those controlling relays, can be put back to their proper state before damage from hot switching can occur.

```
*********************************************************************
 Instrumentation Memory Map:   MemBase =      Group = 0
*********************************************************************
2nd Adx Char ---->   0  1  2  3  4  5  6  7   8  9  A  B  C  D  E  F
1st Adx Char -> 0   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 1   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 2   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 3   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 4   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 5   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 00
1st Adx Char -> 6   48 01 7F F7 10 02 FF 00   20 01 7F F7 10 02 FF 00
1st Adx Char -> 7   4C 01 7F F7 10 02 FF 00   5F 01 7F F7 04 00 00 00
1st Adx Char -> 8   00 29 7D 00 00 00 01 00   00 42 00 00 20 00 01 00
1st Adx Char -> 9   00 18 00 00 00 00 00 00   73 21 7F FF 00 5C 6C 00
1st Adx Char -> A   50 54 45 54 2E 4F 3B 00   00 00 00 00 00 00 00 00
1st Adx Char -> B   3B 04 7F F7 10 00 00 00   57 04 7F FF 04 00 00 00
1st Adx Char -> C   00 84 00 00 00 00 00 00   00 84 00 00 00 00 00 00
1st Adx Char -> D   00 84 00 00 00 00 00 00   00 84 00 00 00 00 00 00
1st Adx Char -> E   00 00 00 00 00 00 00 00   00 7F FF 00 00 00 03 30
1st Adx Char -> F   00 00 00 00 00 00 00 00   00 00 00 00 00 00 00 38
```

Figure 4 - Memory Map of 256, 8-bit Registers

Keeping Control of the Prober

When registers are disturbed within the prober, the best scenario is loss of communication and/or lock-up that requires resetting the machine. Worst case, the chuck is driven in the X or Y direction while the probes are in contact with the wafer. The result is a destroyed probe card and a wafer that might have to be scrapped.

Several steps are taken to reduce sensitivity of the prober. One is to add grounds to the frame and forcer. This prevents them from picking up and re-radiating the RF pulse envelope. Another is to replace older TTL logic control boards with newer ones implemented CMOS logic that are newer, but inherently slower, so the boards are far less susceptible to high frequency noise. In addition, one-shot reset lines on control boards are made less sensitive by placing large (up to 1μF) capacitors on them.

Lastly, the twin-axial chuck bias cable breaks down at <600V. Fortunately, insulation of the chuck from the forcer is adequate for >3kV operation. Reedholm replaces the cable with one used for Reedholm picoammeter applications. The low-noise design of that cable precludes voids in the signal to shield insulation, and the lack of voids results in >3kV strength.

Connecting to Instrumentation

Standard configurations of Reedholm parametric test systems provide dc parametric testing to ±100V and ±550mA. The self-calibration module simplifies dc calibration and conformance to quality assurance programs such as ISO9000 and subsequent versions. The HISMU increases dc currents to ±5A, and the 2kVM provides 0 to +2000V. In addition, IEEE-488 controlled instruments can be connected to the instrument switching system through high quality user function interface modules to address future needs. Prober control is also through the IEEE-488 interface. Figure 5 is a schematic of key elements in the standard RI-2KV/5A.

Guarded Kelvin Switches

System instrumentation (precision current-voltage forcing supplies and current-voltage meters) are connected through guarded/shielded analog pathways, with force and sense lines separated so that voltage can be accurately measured or sensed no matter how far away the device under test might be. Since guards are driven by fast amplifiers, shield capacitance is not a factor for current or capacitance measurements.

Prevention of Hot Switching

Hot switching is the opening or closing of relay switches while potentially damaging currents or voltages are present. Damage is due to contact arcing, and repeated or large arcs lead to welding of the switch contact areas.

Prevention of hot switching dramatically increases reliability of test systems that use reed relay switches, which are required in order to achieve the desired measurement performance through a matrix. If hot switching is prevented, reed switches have lifetimes in the billions of operations, or long enough to last hundreds of years under normal operations.

In Reedholm systems, potential hot switching of instrumentation and matrix connections within applications software is prevented by low-level hardware software drivers, even for user written test functions.

Memory Map Monitoring & Recovery

In addition, the memory map is continuously monitored for uncontrolled state changes during all breakdown tests, not just those involving the 2kVM module. As noted before, rapid communications detect incorrect changes and put relay control registers back to their proper state before damage from opening or hot switching can happen.

MTTF >25000 Hours

Painstaking prevention of hot switching has resulted in extremely reliable test systems. Using returned material authorization (RMA) records, meantime between repairs for systems similar to the RI-2kV/5A is >25000 hours.

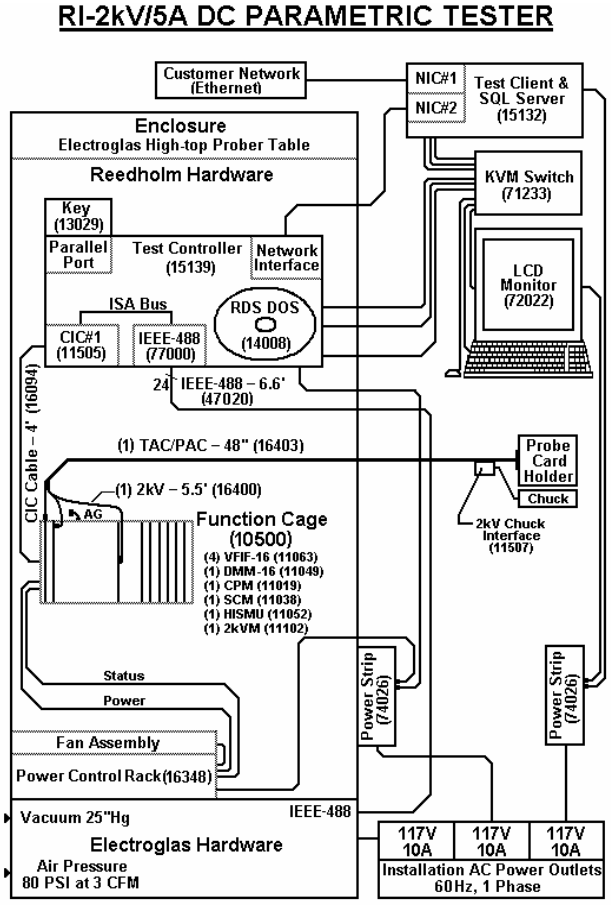


Figure 5 - Schematic of Basic RI-2kV/5A System

Simple Probe Card Interface

Connections are made to a 48-pin rectangular probe card that is removed from the prober in the most convenient manner: top, front, or side. Replacing a probe card is simple. Thumbscrews loosen the probe card clamps, the card is pulled from the connector, a different card is installed, and the screws tightened.

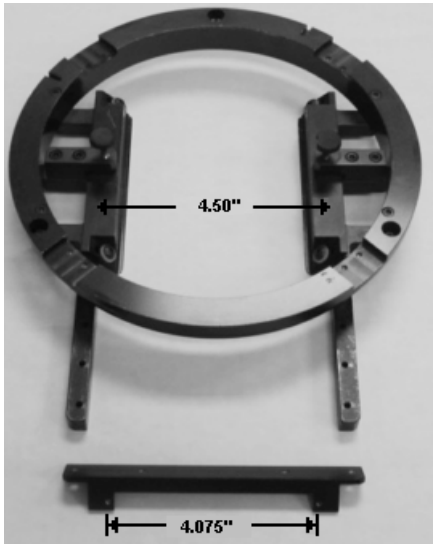


Figure 6 - R&K Probe Card Holder

A typical probe cardholder is shown in figure 6. It is often called an R&K ring, requires a 9.5" opening in the prober, and has been around for >25 years. Almost all rectangular probe cards can be used with this holder. If a probe card of interest is 4.5" wide, it was designed to fit in the R&K design.

The card edge connector of the Reedholm TAC/PAC analog cable is attached to a bracket that is then bolted to the arms of the holder.

Kelvin sensed chuck bias with mini-banana jacks is delivered through an interface box. At high voltage, 2kV relays in the box prevent damaging voltages from reaching matrix pin 8 and the HISMU return.

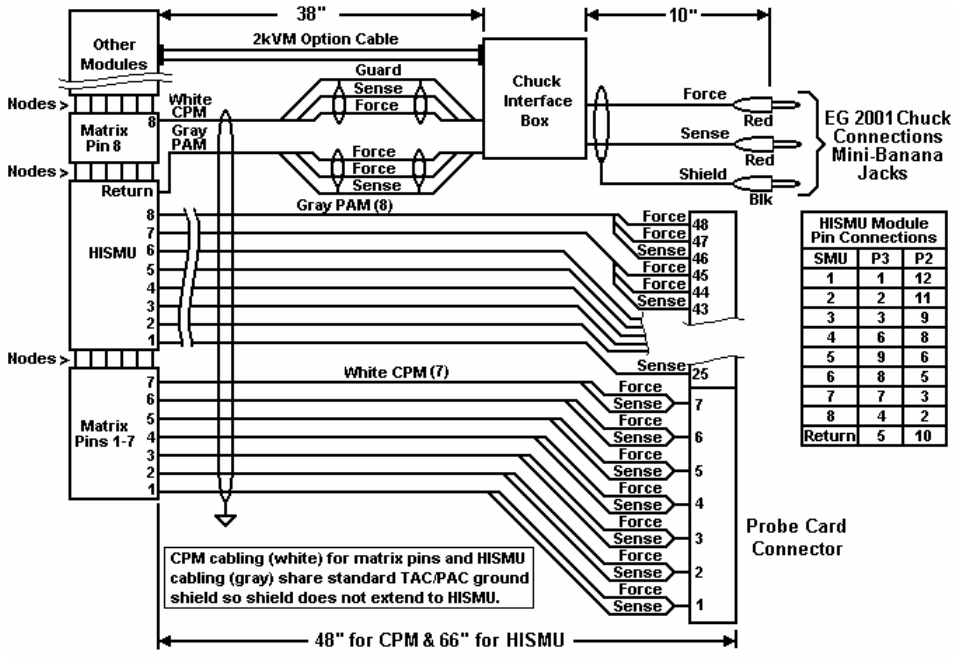
Analog Cabling

A tester and/or prober analog cable (TAC/PAC) brings seven matrix and eight HISMU Kelvin sensed connections to a 48-pin card edge connector. Matrix pin positions 8 to 24 are unpopulated. For higher pin count applications, two matrix modules can be added along with 16 twin-axial cables.

This scheme allows single probe needles for each matrix pin path. Those connect to instrumentation capable of ±100V and ±550mA as well as the HISMU at ±2A through the matrix. In most cases, matrix pin paths are used for base or gate connections. Also, matrix pins are used as return paths for HV breakdown tests.

HISMU pins for currents 0 to ±5A are wired to card edge pins 25 through 48 with two force and one sense connection per HISMU pin. Thus, one HISMU pin can have two probe needles to carry high current and one needle to sense voltage on the wafer. Matrix pin paths can be jumpered on the card to permit continuity checking between needles that are intended to share current.

Care is taken to minimize voltage drop at high currents. Along with the HISMU return wire that delivers drain or collector current, twisted pairs of #24 wire share the emitter or source currents. Sensing is done with the shield of each HISMU cable. Five and a half feet of twisted pair wire at 13Ω/1000ft produces 72mΩ per cable. There could be 20mΩ through the card edge connector and probe card before the probe pins. Thus the resistance per HISMU pin that has to be compensated by Kelvin sensing is ~92mΩ. Resistance is ~200mΩ in the return path due to relay switches in the chuck box, but does affect not drive voltage.



HISMU Module Pin Connections		
SMU	P3	P2
1	1	12
2	2	11
3	3	9
4	6	8
5	9	6
6	8	5
7	7	3
8	4	2
Return	5	10

Figure 7 - RI-2kV/5A TAC/PAC Analog Cable

Rectangular Probe Card

There are several suppliers of high quality, inexpensive rectangular probe cards such as the one shown in figure 8. They only cost a couple of hundred dollars, provide current delivery >5A without compromising low current results, and can be changed in less than a minute. RF probes can be added to the cards as required.

These cards are far less expensive than cards that go into parametric test heads, yet deliver the performance needed for volume testing of high power, vertical devices.

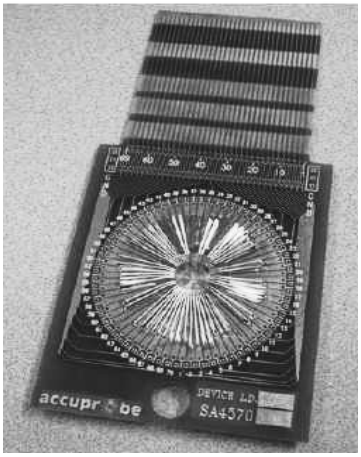


Figure 8 - 4.5" Card with Blades

The widest part of the card is 4.5", and the 48 card edge fingers (24 on each side) are on 0.156" centers. Cantilevered blades are installed on this particular card. Those are the easiest type to maintain, but an alternate epoxy ring approach is more robust. Probe card length can be selected for 75mm to 200mm wafers.

Alternate Cards and Holder

For a nominal fee, the TAC/PAC can be attached to other types of card edge connectors used with rectangular probe cards. A higher charge is made to connect the TAC/PAC to probe cardholder or adapter for circular or other shaped cards.

In such cases, Reedholm modifies two blank cards to provide self-test and training accessories for use at the end of the TAC/PAC.

Savings from Eliminating the Test Head

Test heads with competitive systems are so heavy that an expensive prober is needed just to carry the weight. Instead of a low cost prober that Reedholm can supply, one of those systems results in spending two or three times as much for a prober that is probably much slower and more expensive to maintain. In addition, heavy test heads cannot be handled by an operator, so an expensive manipulator is needed. Lastly, those heavy, bulky test heads require five to ten minutes for probe card change outs.

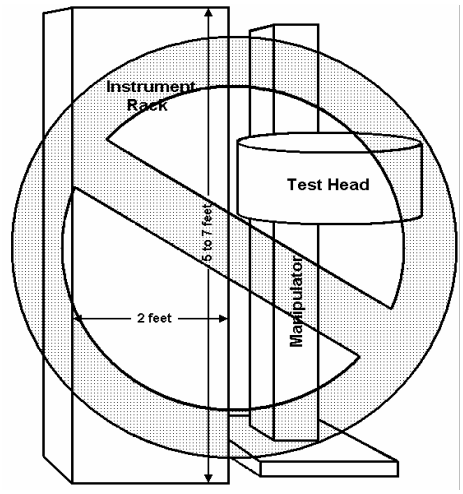


Figure 9 - Floor Space Savings with RI- 2kV/5A

The diagram in figure 9 is roughly to scale for a rack system with test head and manipulator that takes as much floor space as the RI-2kV/5A. In addition, a prober capable of carrying the weight of the test head takes half again as much space as the RI-EG prober.

Assuring System Quality

Accessories and software are provided to assure that the system is working properly without having to infer that from wafer test results.

Not a Collection of "OK" Boxes

With systems built from boxes of instruments and software, there is never enough time to properly document them and creating tools to assure overall system quality is an even lower priority. As a result, there is seldom a way to be sure that the system is behaving beyond instrumentation self test firmware saying "OK".

Preventive System Maintenance

Customers are encouraged to run self test software at the beginning of a shift or when starting a wafer lot because those are convenient times to change a probe card for a loop back accessory that checks the TAC/PAC as well as the instrumentation. In <5 minutes, the diagnostic self test software assures performance to specification for:

- Current leakage
- Open/short testing
- Voltage and current compliance
- Voltage and current accuracy

Independent Calibration Assurance

Unlike instrument boxes that claim internal self-calibration, a separate SelfCal Module (SCM) provides independent confirmation that instrument modules are calibrated. SelfCal takes longer to run than diagnostics, so customers are advised to run it once per quarter.

Fast 2kV Steps Without Overshoot

Fast I-V measurements can be made in a few milliseconds. Figure 10 shows an output plot from sweeping a voltage and measuring current through a 1MΩ resistor. This particular breakdown test measures leakage current at 100V before starting a ramp to 1700V with 50V steps.

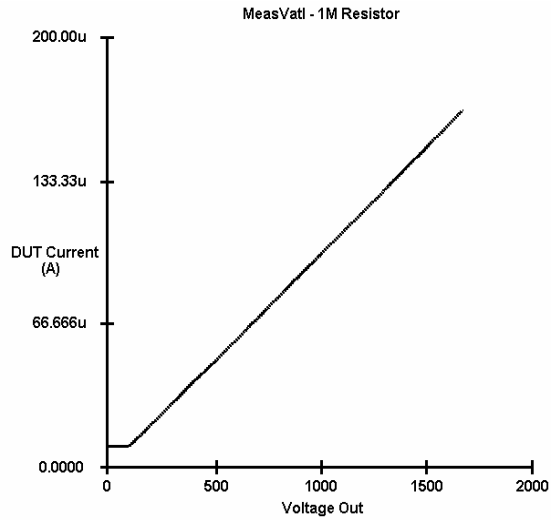


Figure 10 - I vs V Plot for Measure V at I Test

Figure 11 shows test signals using a digital oscilloscope. The top trace is the DMM output on the 1mA range. Each current measurement takes 40µsec. The bottom trace is taken with a 2.5kV probe across the 1MΩ resistor.

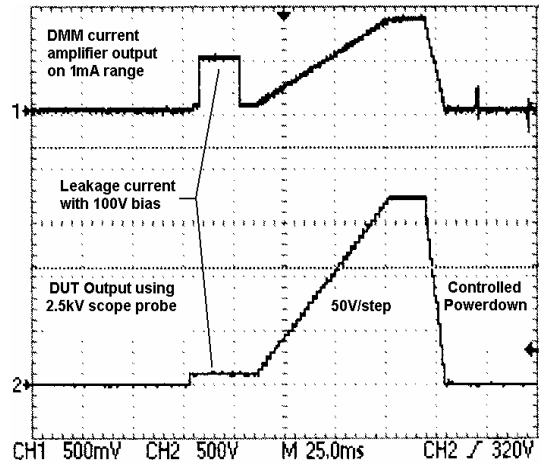


Figure 11 - Biasing Speed at 2kV

The leading edge illustrates the degree of control over test voltage, and the trailing edge shows how quickly the 2kV supply can be changed without overshoot. Note that it took <10ms to change 2kV.

Currents to ±5A

The High Current SMU delivers bias voltages for high current testing and makes current measurements as well. Maximum current is derived from low voltage system supplies so a separate set of supplies is not required. Pulsing duty cycle shown in figure 12 is controlled at the driver level to make sure that ±5A pulses are delivered reliably.

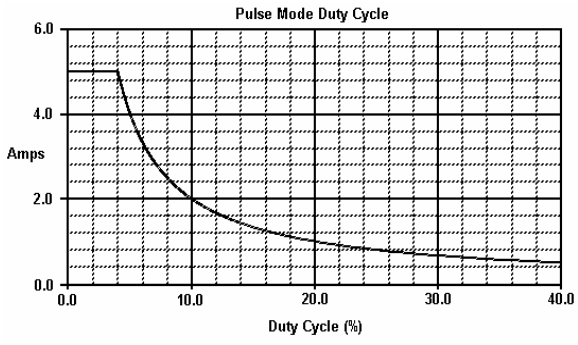


Figure 12 - Duty Cycle for HISMU

Pulse width is settable to 30µs, 100µs, 200µs, or 300µs. Connection to the backplane nodes automatically limits the maximum peak output current to ±2A to protect the node and matrix relays. For the RI-2kV/5A application, auxiliary pins connected to the probe card deliver ±5A. Figure 13 is from a bipolar SIC device using 100µs pulses.

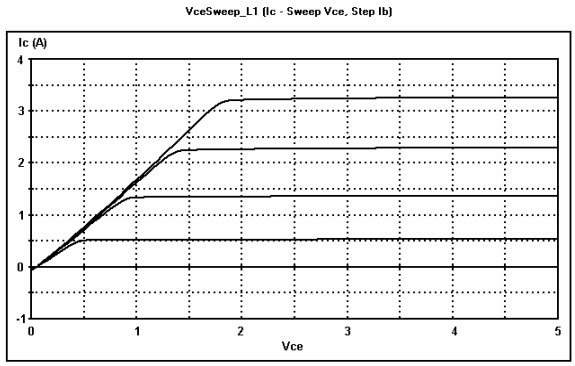


Figure 13 - On-Wafer SIC Bipolar Measurements

Integrated Device Characterization

The WEB user interface provides full control over the tester yet allows it to perform as a curve tracer. It is not necessary to take a wafer to another station to generate characteristic curves like the one in figure 13.

Properly used, this capability eliminates uncertainty about device behavior and what test conditions to use to assure the highest quality data. A curve, or set of curves, can be created for almost every test in table 1.

Software Test Suite

The RI-2kV/5A software suite removes the roadblocks that prevent non-programmers and test system engineers from getting test plans developed, reports generated, and data analyzed. This suite fulfills all requirements of gathering development and production data:

- Test creation for PCM or characterization
- Centralized distribution of test plans
- Test documentation and version control
- Storage and exportation of results
- Reports and graphical analysis of results
- Control of prober and probing patterns
- System integrity insurance and calibration

Test Creation without Spawning Code

As shown in figure 15, RDS Intranet allows tests to be created by simply filling in cells for pins, voltages, currents, delays, etc. However, RDS Intranet does not spew out test code in C or some other language that the test engineer then tweaks and maintains forever.

Data Driven Testing

Instead of generating code, RDS Intranet populates fields in a database record that is downloaded to the test controller and executed in real-time without any delays for interpreting or compiling.

The engineer does not have to learn a programming language, document changes to software, track software, and myriad other tasks needed for proper software control.

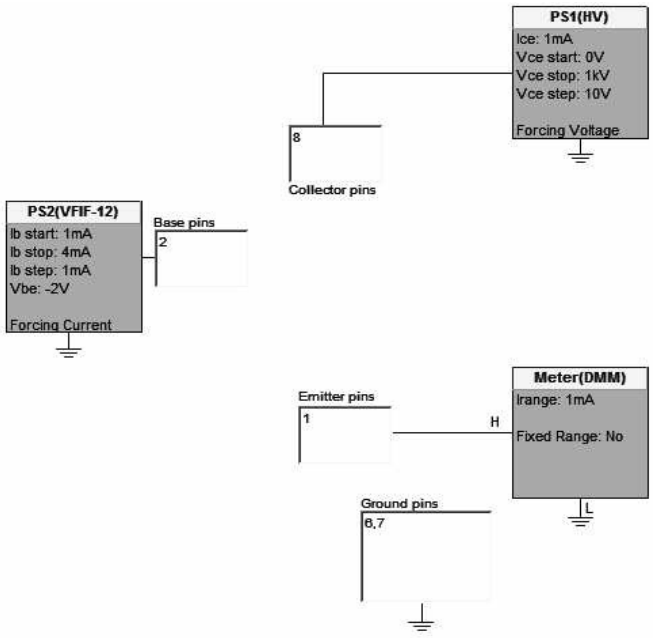


Figure 14 - Schematic Generator

Setting up and controlling test plans is not unlike creating spreadsheet files to manipulate data. Flexibility is more than adequate, yet no one ever asks what language was used to write the spreadsheet program. All that matters is getting results that make sense and that are easily checked when there are yield problems.

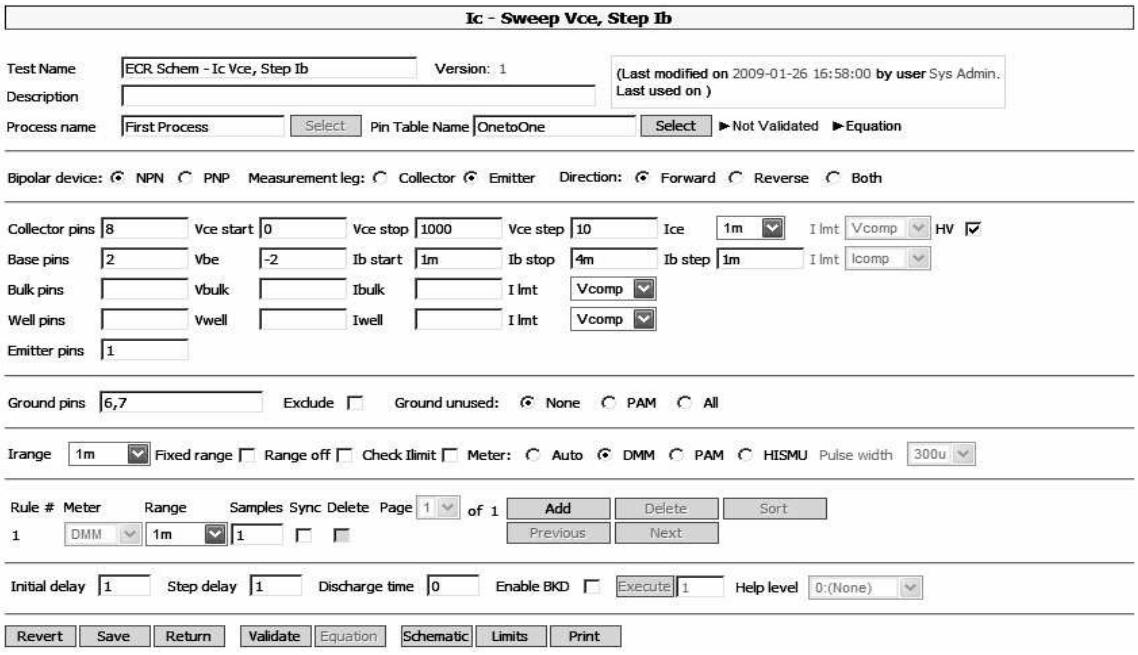


Figure 15 - Input and Edit Test Grid

Feature Rich, Flexible, and no Compiling

No compiling is done, yet very sophisticated software representing man-years of development performs complex calculations in an interactive mode.

RDS Intranet software provides capability well beyond what a test engineer could accomplish starting with source code.

In addition to being used to input a rich set of test parameters, integrated prober control and test storage/manipulation features are also data driven.

Not a Limited Set of "Canned" Routines

"Canned" source code routines frequently lack the ability to test many device permutations, and that is why source code has to be customized. However, the RDS Intranet test engine supports:

- Multiple pins per DUT leg (drain, gate, etc.).
- Biasing and grounding extra DUT pins.
- Forcing voltage or current on extra pins.
- Executing user input equations.
- Using prior test results for test conditions.

After a test is created and found effective, being a record makes it easy to copy and use as the starting point of setting up a new test.

More Than Windows

The Intranet user interface is a WEB application, not just a Windows program. That makes it straightforward to permit database access by all who might need it while still providing security. Thus, a device engineer could answer his or her test questions without having to call a meeting or requesting information from the person with testing responsibility.

No Test Engine Ambiguity

Suspect test data can sometimes be traced to improper test conditions or algorithms. With Reedholm software, algorithms are not subject to uncontrolled tweaking, so valuable time is not spent trying to work backwards through code changes.

Since data used to control testing is in a centralized and controlled database, retrieving it eliminates ambiguity over what test conditions were used for suspect data. Engineers unfamiliar with Reedholm software, but who have critical knowledge about the issue, can be brought into the discussion by using automatically generated test schematics shown in figure 14.

No Compromise on Test Speed

The flat, memory mapped architecture is inherently faster than possible with multiple instruments, each having processors for control. Test code execution speed is as fast as the most optimized version of compiled code. Data driven testing is sometimes misinterpreted as having an interpreter level. But that could not be further from the truth. Data is not moved or modified during software execution, so speed is the same as if data were compiled with the code.

Delays and result averaging to reduce noise are the major reasons for slow testing. Those creep into compiled routines, and programming engineers never seem to have time to take them out. With Reedholm software, delays and averaging are selected with as much flexibility as needed to match what is found with response versus time plots that are unique to Reedholm.

After a test plan is set up for volume testing, reports like that in figure 16 can be generated to identify test speed bottlenecks to review for further speed increases. Inclusive of prober movement, test time per site was 600msec for this SIC wafer tested at 2kV.

Intradie	#	Test_Name	Units	Total	Min Exec	Max Exec	Avg Exec	Total Exec
M1	1	Igd current.vt	Volts	13,500	00:00:00.102	00:00:01.669	00:00:00.147	00:33:08.054
	2	GS BV at 500uA.vt	Volts	13,500	00:00:00.017	00:00:00.060	00:00:00.032	00:07:05.920
	3	Return result at 500uA.vt		13,500	00:00:00.000	00:00:00.000	00:00:00.000	00:00:00.341
	4	BVdsx: Is<1mA, Vds=1650 V.vt	Volts	12,304	00:00:00.096	00:00:00.229	00:00:00.146	00:29:56.911
	6	GS BV at 50uA.vt	Volts	13,500	00:00:00.018	00:00:00.046	00:00:00.021	00:04:42.197
	6	Return result at 50uA.vt		13,500	00:00:00.000	00:00:00.000	00:00:00.000	00:00:00.324
	7	BVdsx: Is<100uA, LotTestTimeReport;1.Test_Name (String)			00:00:00.092	00:00:00.194	00:00:00.111	00:22:11.348
	8	Rds(On).vt	Ohms	13,500	00:00:00.019	00:00:00.046	00:00:00.020	00:04:30.057
	9	Id(ON).vt	Amps	13,500	00:00:00.020	00:00:00.021	00:00:00.020	00:04:34.943
	10	Ids at Vgs=-3 V, Vds=2 V.vt	Amps	13,500	00:00:00.021	00:00:00.023	00:00:00.022	00:05:00.492
	11	Ids at Vgs=-8 V, Vds=2 V.vt	Amps	13,500	00:00:00.018	00:00:00.020	00:00:00.019	00:04:18.246
	12	Ids at Vgs=-10 V, Vds=2 V.vt	Amps	13,500	00:00:00.017	00:00:00.046	00:00:00.018	00:04:05.063
	13	Igl current.vt	Amps	13,500	00:00:00.017	00:00:00.044	00:00:00.018	00:03:59.278
	14	Vth @ Vds=10 V, Id=100uA.vt	Volts	13,500	00:00:00.041	00:00:01.238	00:00:00.046	00:10:14.582
	15	Vth @ Vds=1 V, Id=100 uA.vt	Volts	13,500	00:00:00.045	00:00:01.241	00:00:00.048	00:10:51.877
	16	Delta Vth.vt	Volts	13,500	00:00:00.000	00:00:00.028	00:00:00.000	00:00:03.004
							Total Test Time:	02:24:42.839

Figure 16 - Test Time Report from Acquire

One to Many Linking

Using a test in more than one list is simple because each test is a database record that can be linked and used in any number of test lists. Maintaining test lists across many process formulas and products is simplified when a test only has to be changed once for the new version to be applied everyplace it is used.

This attribute of linking one to many is extended to test lists, probe patterns, report options, pass-fail settings, etc.

Data Storage and Extraction

During training, the engineer tasked with bringing the RI-2kV/5A tester on-line is shown how to input test data, investigate and optimize results, and control the prober. What he or she does not have to do is figure out what to do with test data. That is, decide:

- Where to store?
- What format to use?
- How to provide access?

These questions are moot because all data is in an SQL Server database accessed directly or with Reedholm reporting and analysis tools, one of which is the wafer map shown in figure 17.

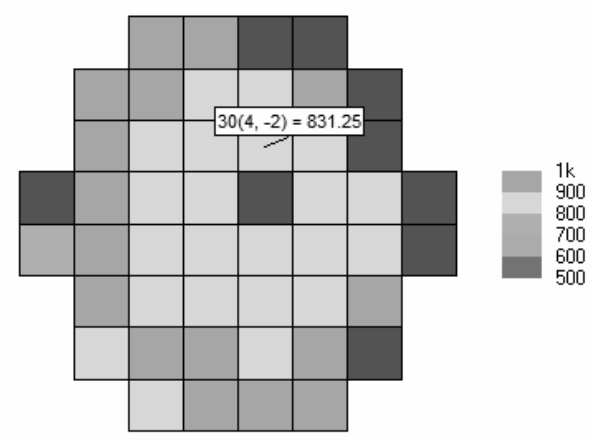


Figure 17 - Examine Wafer Map

Exporting Data

In addition, data can be automatically exported in CSV (flat ASCII) and XML file formats compatible with most spreadsheets, databases, and analysis packages.

Many Reedholm customers use Excel® to augment the Crystal Reports package provided with each system and that Reedholm used to generate standard lot and wafer reports.

Partial List of Test Types

Beta at an Ib, Ic, or Ie
Calculate Delta Length
Current at a Voltage
Early Effect
4 Terminal Voltage, Resistance, or van der Pauw
gm or Vt at an Ids or % of Ids
gm or Vt at a Two Drain Currents
gm or Vt at a Two Gate Voltages
gm or Vt at PMS
High Voltage (+2kV) Capacitance
High Voltage (+2kV) Continuous Breakdown
High Voltage (+2kV) Snapback Breakdown
Ic - Sweep Vce, Step Ib
Ic - Sweep Vce, Step Vbe
Ic and Ib - Sweep Vbe
Ids - Sweep Vds, Step Vgs and Vbs
Ids - Sweep Vgs, Step Vbs
Ids - Sweep Vgs, Step Vds
Ids at a Vgs
Isub - Sweep Vgs, Step Vds
Measure Capacitance
Measure Capacitance - Sweep +2kV
Measure Capacitance - Sweep V
Measure Current
Measure Current - Sweep Time
Measure Current - Sweep Voltage
Measure Current at High Voltage (+2kV)
Measure Resistance - Low Bias
Measure Resistance - Sweep Voltage
Measure Resistance at Current
Measure Resistance at Current (+200V)
Measure Resistance at Voltage
Measure Voltage
Measure Voltage - Low Bias
Measure Voltage - Sweep Time
Measure Voltage (+200V)
Peak Beta
Replace Parameters with Results
Return Other Result
Saturated Vt
Small Signal Beta
Standalone Equation
Step Voltage Until Current
Stress at a Vgs
Stress Current
Three Terminal Voltage or Resistance
Two Terminal Resistance - Force Current
Two Terminal Resistance - Force Voltage
User Written Test
Vgs at a an Ids or % of Ids
Vgs of Peak Isub
Voltage at a Current (+200V)
Voltage at a Current (±100V)

Table 1 - Subset of Available Test Types

Comprehensive Training and Support

Acceptance and User Training

System performance to specifications is done at Reedholm before shipment. In addition, customers are encouraged to run correlation wafers so that system or training issues can be handled before shipment.

Thus, a major target of system training is to have users ready by end of training populate test plans and set up probing patterns. While system training can be done on-site at an additional charge, doing it at Reedholm minimizes interruptions and maximizes learning. User training covers:

- Building test plans and probe patterns.
- Device characterization and test optimization.
- Data analysis and database maintenance.
- Basic system maintenance.
- Importing DOS test plans if upgrading.

Documentation

After the system is installed, on-line user manuals describe instrumentation and application software operation down to the bit level. The manuals can also be accessed on the installation CD for those rare circumstances when the application does not start.

Real-Time Hands-on Assistance

Applications assistance is provided via the Internet using GoToMyPC software. With it, Reedholm engineers can control a system anywhere in the world to:

- Run maintenance programs.
- Troubleshoot device test issues.
- Apply software patches.

In addition, telephone and e-mail support is available from the U.S. Monday through Friday, excluding holidays at:

- Phone: 1.512.876.2268
- Email: support@reedholmsystems.com

Local technical support from Reedholm distributors is also available in many parts of the world.

Warranty

Warranty is 12–months for defective parts and labor with work performed at the Reedholm Texas facility.

For remote facilities that cannot use overnight shipping effectively, a set of spares is an economical solution to minimizing downtime. Spares also reduce downtime that occurs when custom agents get involved.

Extended warranty and service contracts are available. However, service contracts are seldom justified for systems with demonstrated MTTF >25000 hours.

Alternatively, an open purchase order allows a test engineer to get someone from Reedholm on-site without having to wade through lengthy approval delays.

Automated DC Calibration

The Self Calibration Module (SCM) provides an easy, cost-effective method of making Reedholm instrumentation traceable to corporate voltage and resistance standards. An accurate, stable voltage reference coupled with an instrument grade high voltage amplifier provides precision currents and voltages for all of the instruments provided in the standard RI-2kV/5A: VFIF-16, DMM-16, and HISMU. The 2kV module software provides automatic calibration without the SCM. In addition, the SCM is used to calibrate optional modules such as the HVSMU, which provides ±250V span, and the PPG-4, a module with fast, nested pulses well suited for NVM characterization.

In operation, the SCM is used to generate offset and gain error correction factors for dc instruments, after which the factors are used to prevent source errors and to compensate for measurement errors. As long as the self-calibration software can correct module accuracy, the module meets its accuracy specifications.

SCM Transfer Accuracy (24 Hr, ±2C°)

Voltage Range (V)	Error (% of Value)	Current Range (A)	Error (% of Value)
0.25	0.05	100n	0.04
0.50	0.03	1µ	0.02
1.00	0.02	10µ	0.02
2.50	0.01	100µ	0.02
5.00	0.01	1m	0.02
10.0	0.01	10m	0.02
25.0	0.01	100m	N/A
50.0	0.01	1	N/A
100	0.01		

2kVM Voltage Accuracy/Calibration

The 2kV module outputs a stable voltage from 0 to 2000V by converting a current supplied by a VFIF serving as a precision current source. Within the chuck bias box, 2kV relays isolate lower voltage paths when the 2kV module is being used. Also within the box are a precision 100:1 divider and a 100kΩ output resistor string. The divider permits measurement of output voltage by the system, and the output string limits discharge from cable capacitance during destructive device breakdown.

To maximize voltage accuracy, the transfer function of the 2kVM (current to voltage conversion ratio), divider ratio, and output resistance are measured and stored in a text file during software calibration. To start calibration, a manual switch is thrown on the chuck interface box and 2kVM calibration is selected from a pull-down menu.

Since measurements are done with the system DMM and VFIF modules, accuracy of the 2000V output is bootstrapped to be the same as those two modules, so errors are nominally <0.05%.

Specifications

Instrument specifications apply at the end of the TAC/PAC analog cable without a probe card attached. Some commonly used wafer test accessories (especially probe cards) reduce parametric testing accuracy at low currents. Care is needed in designing the test environment to achieve maximum performance.

Use Conditions

Temperature: 18°–28°C
Humidity: 30%–50% R.H. Non-Condensing

Nominal Power: 117V, 50 or 60Hz

Regulated supplies isolate instrumentation from power line variations of more than ±10%. Voltages different than nominal are addressed with step up or step down transformers.

Basic Switching System

Specifications for low noise, high performance matrix switching apply to user function interface modules as well as the CPM and node switches of instruments.

1) Maximum Stand-off Voltage: ±600V
2) Maximum Carrying Current: ±2A
3) Leakage Resistance: 1 x $10^{12}\Omega$/System Pin Count
4) Pin-to-Pin Thermal EMF: <±100µV Max
5) Pin-to-Pin Resistance (shorted): <400mΩ
6) Switching Speed (including software delay): 1ms

VFIF-16 (P/N 11063)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Voltage	2.5V	250µV	0.03	78.125µV
	5V	500µV	0.03	156.25µV
	10V	1mV	0.03	312.5µV
	25V	2.5mV	0.03	781.25µV
	50V	5mV	0.03	1.5625mV
	100V	10mV	0.03	3.125mV
Current	100nA	125pA	0.20	1.5625pA
	1µA	125pA	0.15	15.625pA
	10µA	500pA	0.05	156.25pA
	100µA	5nA	0.05	1.5625nA
	1mA	50nA	0.05	15.625nA
	10mA	500nA	0.05	156.25nA
	100mA	5µA	0.05	1.5625µA
	1A	50µA	0.10	15.625µA

Comments:

1) Specifications apply for 24 hours and ±1C° after SelfCal or manual calibration.
2) Current specifications apply up to 200mA. Limit occurs at approximately 240mA.
3) CMRR: In current mode, <0.0002% of range per volt of output
4) Accuracy on lowest two current ranges is measured with line cycle integration.
5) Current accuracy on a given range has uncertainty of ± (offset error + % of value error). For example, forcing 100µA on the 100µA range results in:
   I_{out} = 100µA ± (5nA + 0.05% of 100µA)
   I_{out} = 100µA ± 55nA
6) Voltage accuracy uncertainty is ± (offset error + % of value error). For example, forcing 1V on the 2.5V range results in:
   V_{out} = 1V ± (78µV + 0.03% of 1V)
   V_{out} = 1V ± 378µV

Digital Multimeter (P/N 11049)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Voltage	250mV	250µV (50µV)	0.03	7.8125µV
	500mV	250µV (50µV)	0.03	15.625µV
	1V	300µV (75µV)	0.03	31.25µV
	2.5V	500µV (100µV)	0.03	78.125µV
	5V	1mV (200µV)	0.03	156.25µV
	10V	2mV (400µV)	0.03	312.5µV
	25V	5mV (1mV)	0.03	781.25µV
	50V	10mV (2mV)	0.03	1.5625mV
	100V	20mV (4mV)	0.03	3.125mV
Current	100nA	100pA	0.20	3.125pA
	1µA	300pA	0.15	31.25pA
	10µA	2nA	0.05	312.5pA
	100µA	20nA	0.05	3.125nA
	1mA	200nA	0.05	31.25nA
	10mA	2µA	0.05	312.5nA
	100mA	20µA	0.05	3.125µA
	1A	200µA	0.10	31.25µA

Comments:

1) Specifications apply for 24 hours and ±1C° after SelfCal or manual calibration.
2) Maximum output current on 1A range is ±350mA. On other ranges, maximum is 125% of range.
3) Settling time to 0.01%:
   4.0ms, 100nA Range
   2.3ms, 1µA Range
   1.7ms, 10µA-1A Ranges
   1.6ms, 250mV-100V Ranges
4) CMRR Voltage:
   5µV/V (106dB)
5) CMRR Current::
   1 ppm of range per volt, 10µA -1A
   2 ppm of range per volt, 1µA
   6 ppm of range per volt, 100nA
6) Accuracy of the lowest three current ranges is determined with digital averaging approximating line cycle integration.
7) Accuracy of current measured on a given range is proportional to range and a percentage of current being measured. For example, measuring 50µA on the 100µA range would have uncertainty of:
   50µA ± (20nA + 0.05% of 50µA) = 50µA ± 45nA
8) Range offset errors shown in parentheses () apply for an eight-hour period after auto zero and for ±1C°.
9) When measuring currents from sources with non-zero output conductance, the following is added to the error specifications:
   ±(830 ppm of value +151µA)/mho

HISMU (P/N 11052)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Current	10A	2.5mA	0.10	2.5mA
Voltage	2.5V	2.5mV	0.05	1.25mV
	5V	5mV	0.05	2.5mV
	10V	10mV	0.05	5mV

Comments:

1) Analog settling time is <5µs to within 0.1%.
2) Pulse width uncertainty is <1µs.
3) Accuracy of voltage forced on a given range is a function of the range offset error and the value forced, for example, forcing 1.25V on the 2.5V range results in:
   V_{out} = 1.25V ± (2.5mV + 0.05% of 1.25V)
   V_{out} = 1.25V ± 3.125mV
4) Accuracy of current measured is a function of the range offset error and the value measured, for example, measuring 1A on the 10A range results in:
   I_{out} = 1A ± (2.5mA + 0.1% of 1A)
   I_{out} = 1A ± 3.5mA□