Current Stress Module

[ISM]

- **±100V Compliance Voltage**
- **±100mA Output Current**
- **10W Output Power**
- **Programmable Bipolar Current & Voltage**
- **10mA & 100mA Current Ranges**
- **Low Quiescent Current**

Analog Circuitry

The ISM is a programmable current source which can supply a load current of ±100mA at a compliance voltage of ±100VDC. Its analog circuitry consists of two precision DACs, an error amplifier, a precision voltage clamp, a voltage-controlled current source (VCCS), a power output stage, a sense buffer amplifier, and precision feedback components. The block diagram is shown in Figure 1.

Output Voltage

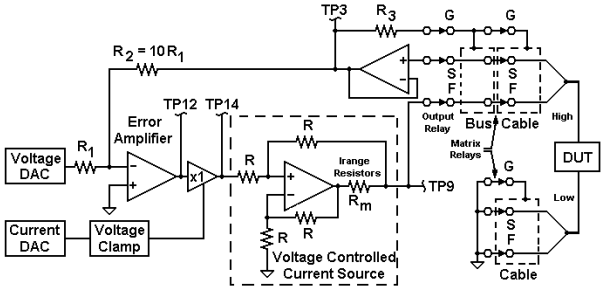

Figure 1 - ISM Block Diagram

The error amplifier provides sufficient gain in the control loop to ensure that its negative input will remain at virtual ground unless the load current attains the programmed limit level. Thus, for the condition of no current limit, the ratio R_2/R_1 and the VDAC determine the output voltage. The VDAC is a 12-bit precision device that outputs voltage between -10V and +10V.

Specifications ($18°C \leq T_A \leq 28°C$)

Mode	Range	Source Error		Resolution
		Offset	% of Value	
Compliance	100V	100mV	0.05	50mV
Current	10mA	5µA	0.05	2.5µA
	100mA	50µA	0.05	25µA

Comments:

1. CMRR: <0.002% of range per output volt in current.
2. Accuracy of current forced in a given range is a function of range offset error and the value forced, i.e., ± (Range error + percentage of value error).
   For example, forcing 10mA on the 10mA range:
   10mA ± (5µA + 0.05% of 10mA)
   10mA ± 10µA

Voltage-Controlled Current Source

Within the VCCS are two precision resistors which correspond to the two current ranges and determine the transconductance of the VCCS. The maximum output current is determined by the product of the IDAC output voltage and the VCCS transconductance

Output Current

The reference for the bipolar voltage clamp is produced by the 12-bit precision IDAC which outputs a programmable voltage between 0V and 5V. That in turn ensures that the input to the VCCS can never exceed the magnitude of the IDAC voltage in either polarity. Therefore, the maximum output current is proportional to the IDAC level.

Sense Buffer

The sense buffer ensures that the compliance voltage will exist at the DUT for the condition of no current limit even if voltage is dropped down the force (F) line. It also ensures that all of the VCCS output current flows to the DUT because no current can flow down the sense (S) line. In addition, the sense buffer serves to drive the output guard through R3.

Current Step Response

The ISM output current step response is independent of range as shown in Figure 2 on the next page. Step-response time for non-zero load resistance exceeds the time shown in Figure 2 with a time constant directly related to the product of the load resistance and the load capacitance. The left curve in the figure uses the left scale and the right curve uses the expanded right scale.

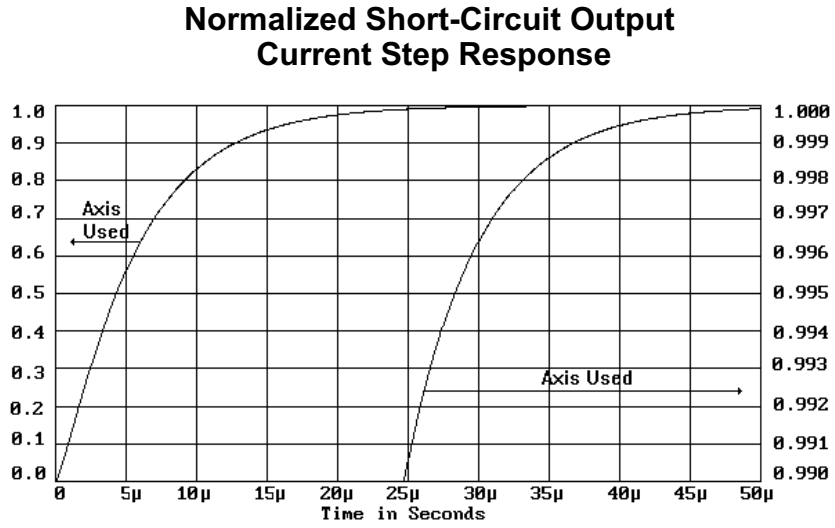

Figure 2 - 10mA and 100mA Ranges