PHYSICS NOTE

PN-101

Process-Induced Charge Damage Physics

Introduction

In addition to other processing effects, thin oxides can be electrically altered by subsequent wafer process steps in at least two ways [1]-[2]:

- Capture of carriers injected into the oxide by uncharged trap sites. The resultant increase in trapped charge can alter threshold and gain.
- Surface to substrate potentials capable of injecting carriers create defects which lead to early wearout.

Driving Forces Behind Damage

Plasma based processes are a major cause of process induced charge damage. Through creation of a plasma above the wafer surface, ion implantation is another major cause. Plasmas inject carriers into oxides through UV radiation and Fowler-Nordheim tunneling caused by surface to substrate potentials. A charging potential capable of Fowler-Nordheim tunneling is also capable of trap generation [3].

It is generally agreed that process induced damage is due to the same mechanisms which cause damage in time dependent dielectric testing. There has been considerable modeling in the past three years on the forces behind charge damage. The model in Figure 1 was developed by Vella [4] and verified using direct measurements with CHARM^{TM} wafers.

In the Vella model, I_P is due to implant ions including effects of secondary electron emission, I_B is due to slow positive ions, and I_E is due to plasma electrons. I_D is the sum of all three components. V_D is the maximum voltage which would occur if no current flowed through the device. Current due to plasma electrons is highly dependent on surface to substrate voltage, and acts to clamp the peak voltage. The clamping effect is shown schematically in Figure 1 using an ideal diode in series with a source of V_D volts. Thus, when the gate to substrate voltage reaches V_D, gate current is also clamped, and any increase in I_D is shunted away from the gate.

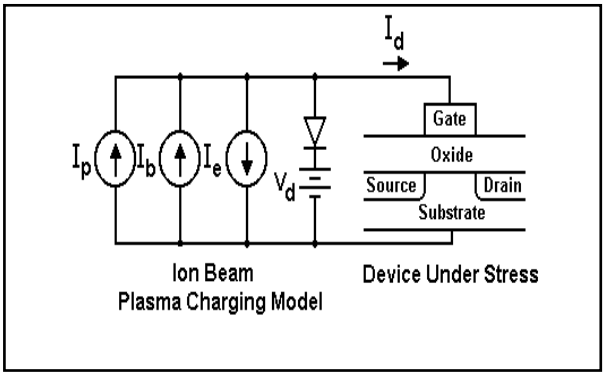

Figure 1 - Vella Model

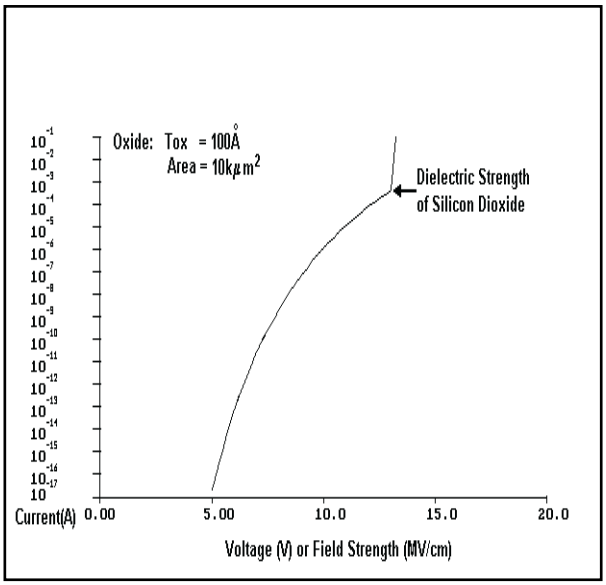

Figure 2 - Idealized F-N Plot

Causing Damage

If V_D in Figure 1 is low enough, i.e., below 5MV/cm, traps are not generated [6]. The reason can be seen from Figure 2, an idealized plot of Fowler-Nordheim tunneling for a 10,000μm^2, 100 angstrom thick oxide capacitor. Notice that current flow at 5MV/cm would be less than 10^{-17} amperes, a level which could be sustained for years with no degradation.

Current Multiplication - The Antenna Effect

A gate oxide can be damaged even when it is not being patterned or deposited. Conducting layers attached to the gate can couple currents from process steps occurring well after gate processing. In addition, conductors attached to a gate act as a current collection antenna multiplying total gate current well above that implied by gate area. Thus, computation of possible damage current needs to take into account the total gate conductor area which can intercept plasma current.

Failure Mechanism

Dumin et al [3] postulated a physical model for thin oxide wearout which not only fit their experimental data, but resolved seemingly conflicting data previously published by other authors. Subsequently, Schlund et al [6] published a similar model based on the "formation and coalescence of vacancy defects."

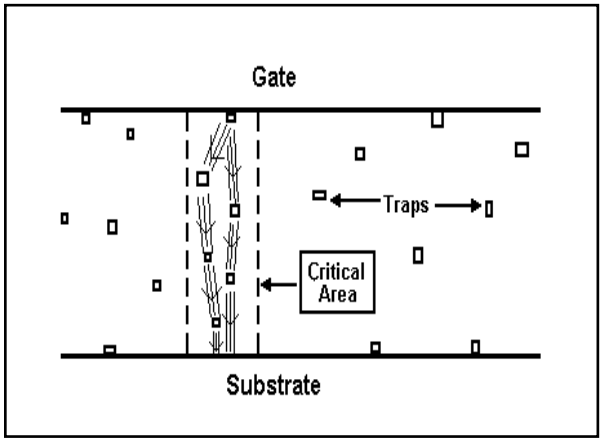

Figure 3 - Traps Lead to Localized Failure

The Dumin model observes that generation of oxide traps in thin oxides (< 100 angstroms) is due to high field induced tunneling from structural weaknesses. Thicker oxides might have some trap generation due to impact ionization, but there are reasons to doubt that electrons accelerated by the field have much of an effect on total trap creation.

When enough traps are generated that line up from gate to substrate within a small enough volume (as shown by the critical area in Figure 3), physical failure occurs due to thermal runaway from localized heating. Figure 3 is based on the Dumin paper.

Testing Considerations

During testing, damaged oxides typically exhibit much lower than normal voltages when low level current is forced through them. Thus, departure from voltages predicted by tunneling models indicates plasma damage. Another indication of damage is a difference in transistor operating parameters between a device with no antenna and devices with antennas.

Annealing of gate oxide damage through subsequent processing can mask damage [2]. In some cases, damage can be revealed through stressing with a higher level current. Thus, a sequence of "test-stress-test" reveals damage through changes in device parameters.

However, very thin oxides sometimes exhibit a quasi-breakdown condition which effectively protects the oxide from further damage and minimizes shifts due to a specific stress current. In such cases, it has been recommended [8] that a constant voltage stress be used to uncover damage.

CHARM Testing

CHARge Monitoring (CHARM) is a relatively new method that uses specialized test wafers to measure surface to substrate potential and current density, the driving forces behind charge damage. Use of CHARM complements damage measurements, but doesn't replace them.

CHARM wafers consist of EEPROM's with associated circuitry to allow charge potentials to be stored and measured just as test wafers are used in-line. Resulting wafer maps indicate variation of charging parameters (potential, polarity, flux) across the wafer [9].

References

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