# PHYSICS NOTE

PN-103

# Field-Induced Thin Oxide Wearout

## Introduction

Under voltage stress, the insulating quality of a thin oxide degrades due to generation of defects. If defects align themselves sufficiently through the oxide, and if the applied voltage is high enough, localized current density produces enough heat to transform the oxide from an insulator to a conductor.

Besides defects introduced during manufacturing, bulk and interface defects are generated through electric field stress and injection of hot carriers. This note is concerned with wearout due to electric field stress encountered in normal device operation. Hot carrier injection is covered in a different Reedholm WLR physics note.

Besides device operation, oxides are subjected to other sources of electric field stress. Process induced charge damage is a common one which is also discussed in a different Reedholm WLR physics note.

Another source of high field stress is electrostatic discharge (ESD). Although guarding against ESD is an important consideration, ESD protection is a design issue considered outside the purview of Reedholm WLR documentation.

## Wearout Characterization Background

Deterioration with eventual shorting of gate oxides has been a serious reliability concern of IC manufacturers for a long time. The generic name for oxide wearout is time dependent dielectric breakdown (TDDB). Until recently, failures were treated symptomatically and monitored statistically. Accelerated testing of oxide reliability has been practiced for almost twenty years. Crook published a method to accelerate TDDB for reliability screening during a time when process induced defects seriously affected device yield [1]. Within a couple of years, Berman [2] justified use of voltage ramps, with some as quick as 10ms, instead of the constant voltage stress used by Crook. Screening was still the main goal.

## Extrinsic and Intrinsic Behavior

Failure plots of breakdown voltage for thin oxide test structures essentially exhibit bi-modal lognormal statistical behavior with dramatically different breakdown voltages for 50% ($t_{50}$) of the failures in each mode. As the mode with the highest $t_{50}$ exhibits breakdown voltage comparable to $SiO_2$ dielectric strength, it is standard practice is to say that mode exhibits intrinsic behavior. The analogy to semiconductor terminology is carried further by naming the mode with lower $t_{50}$ extrinsic and postulating that defects have been introduced into it.

Meyer and Crook [3] made use of the log-normal relationship in developing a newer screen for oxides that purportedly did not cause aging since it isolated the extrinsic mode. Subsequently, there are others who argue for Weibul and other types of distributions; all segregate extrinsic from intrinsic behavior.

In 1994, Dumin et al. [4] proposed a physical model for TDDB which integrated some seemingly contradictory observations and cast doubt on some rather well established beliefs. One of them was that most failures termed extrinsic are

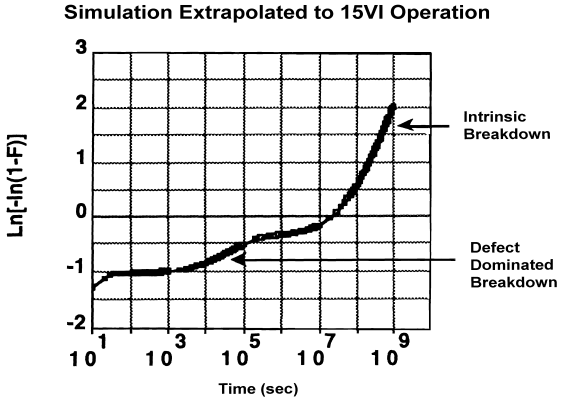


Figure 1 - Simulated TDDB Plot

no different than intrinsic failures. Nafria et al. [5] shed further light on problems with intrinsic and extrinsic classifications.

Through application of the Dumin wearout model, the distribution shown in Figure 1 was simulated. It should be noted that no "extrinsic" population was introduced. For a multi-mode distribution, enough traps needed to be created through voltage stressing and random placement of traps throughout the oxide.

## Oxide Tunneling Current

Fowler-Nordheim tunneling physics based on electron emission from a metal into a vacuum is applicable for emission into $SiO_2$. Lenzlinger and Snow [6] showed that tunneling current flow was electrode and not field dependent. However, the level of current was an order of magnitude lower than predicted. Nissan-Cohen et al. [7] addressed the discrepancy by:

- accurately assessing electrical oxide thickness.
- determining field reduction due to trapped charge.

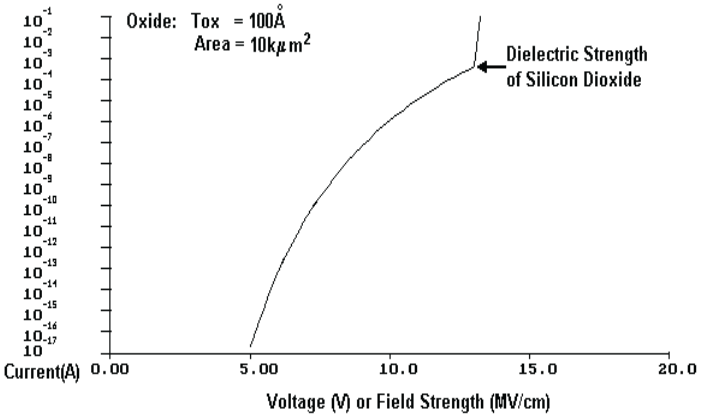


Figure 2 - Tunneling Current

There is general agreement that eventual shorting of an oxide is due to very high current densities within a small volume. Melting point temperatures within oxides can be quickly reached because surrounding undamaged oxide is a good heat insulator.

Figure 2 is a tunneling current plot for an ideal 10nm oxide. Failures can occur at any current shown on the plot, although the probability of failure is higher at higher currents. Thus, the extremely low current density of $10^{-17}$A at 5V may intuitively seem inadequate to cause melting point temperatures, yet that is exactly what happens during oxide TDDB testing.

## Use of $Q_{bd}$ for Oxide Reliability

Given that tunneling current leads to failure, it is logical to assume that damage within an oxide is also caused by tunneling current. One consequence of such an assumption is use of charge to breakdown ($Q_{BD}$) as a measure of oxide reliability. While Weber and Brox [8] published a typical value of 10C/cm$^2$, $Q_{BD}$ has not proven to be a process independent reliability parameter. However, it has generally correlated to TDDB for specific processes under specific test conditions.

Lack of consistency in $Q_{BD}$ results seems to have led to some contradictions. For instance, Turner's explanation of oxide wearout [9] claims that $Q_{BD}$ increases with stress current. On the other hand, Uraoka et al. [10] showed that $Q_{BD}$ degrades at higher current levels. Since Uraoka's paper included data while Turner's had none, and since Uraoka's work also combined optical measurements with electrical ones, it is difficult to support Turner's claims. Incidentally, Uraoka showed that uniformity of current flow through an oxide and $Q_{BD}$ were both degraded for current densities >10mA/cm$^2$. Other than Turner's, there doesn't seem to be any published contradictions of the Uraoka data.

Other reports of $Q_{BD}$ dependence are not so easily reconciled. Apte and Saraswat [11] provide a survey of results in their paper on correlation of trap generation with $Q_{BD}$.

- There can be 2:1 or 3:1 differences in $Q_{BD}$ for the same sample set depending on voltage polarity even with accommodation for work function differences.
- For a given field strength, $Q_{BD}$ is a strong function of oxide thickness.
- Even though tunneling is not strongly temperature dependent, $Q_{BD}$ is highly dependent.

Other papers on oxide wearout besides Apte's argue for use of trap generation measurements for oxide reliability evaluation. Lisenker [12] proposes an index for gate oxide integrity based on the rate of electron trapping after a critical current density is reached. Both Apte and Lisenker correlated trap generation with $Q_{BD}$.

Although $Q_{BD}$ is not ideal for predicting TDDB, it is a superior predictor of transistor parameter degradation. Fishbein and Jackson [13] results indicate that degradation is due solely to total injected gate charge independent of frequency and duty cycle.

## Damage Not Due to Tunneling Current

Creation of traps in the oxide, whether positive, neutral, or negative, leads to oxide failure [4, 5, 8, 11, 12]. Regardless of how traps are formed, when electrons are trapped, the field internal to the oxide is decreased thereby reducing current at a given external voltage stress. If holes are trapped, the internal field is increased leading to higher current flow [12].

Given the heating effect of oxide current, it is tempting to assume that atomic bonds within the oxide and at oxide interfaces can be broken when highly energetic electrons collide with them. Such broken bonds would then be capable of trapping holes or electrons [8, 9, 11]. In fact, Turner's entire explanation of wearout is based on electrons breaking bonds in the bulk and at the interfaces. Recent publications point out the error of that assumption from logical and mathematical viewpoints.

Dumin et al. [4] identifies several contradictions which cast serious doubt on impact ionization by energetic electrons being a significant cause of trap generation.

- Trap generation should be highest near the anode since tunneled electrons have been accelerated across the entire oxide thickness. However, breakdown is dominated by asperities at the cathode, not the anode. Also, trap densities near the cathode are higher than those at the anode.
- Since energetic electrons would travel further in thicker oxides, there should be a thickness dependence on TDDB which does not exist.
- There should be no traps created within tunneling distance of the cathode, yet there are many.
- Interface trap generation should be proportional to cumulative electron flow, or fluence, but is not.
- Breakdown voltage should increase with temperature for impact ionization, yet it decreases.

Besides Dumin's logical reasons for eliminating impact ionization as a significant cause of trap generation, Schlund et al.[14] published mathematical proof that impact ionization could only be a significant damage factor for very high fields. Table 1 is a condensed version of the table from their paper. Note that dipole interaction is the dominant term consistent with Dumin's observation that it is localized high fields which lead to oxide damage, and that tunneling current is simply another manifestation of electric field strength.

In their paper, Schlund et al. [16] provide data supporting the observation that tunneling current only becomes a factor when electric field strength is greater than 11.7MV/cm.

| | Field Strength in MV/cm | | |
|---|---|---|---|
| | 5 | 10 | 12 |
| Mechanical Stress(eV) | $14x10^{-6}$ | $14x10^{-6}$ | $14x10^{-6}$ |
| Thermal Energy(eV) | 0.137 | 0.137 | 0.137 |
| Electrical Energy(eV) | 0.0012 | 0.0049 | 0.0070 |
| Dipole Interaction(eV) | 4.59 | 9.18 | 11.0 |
| Electron Trapping(eV) | 0.0009 | 0.0009 | 0.0009 |
| Tunneling Current(eV/s) | $9x10^{-23}$ | 0.977 | 122 |

Table 1 - Energy Contributions to Damage

## Destructive Phase of TDDB

As yet, there has not been a universal acceptance of results shown in Table 1. There are proponents of hole generation and transport, hydrogen liberation, etc., all of which may play a role in TDDB. As pointed out by Nafria et al. [5], oxide failure is a weakest link one which permits contribution by more than one effect.

However, there seems to be general agreement on final failure from thermal runaway. Others [11, 16] use an illustration similar to that of Dumin [4] in Figure 3 showing growth of a chain of defects or traps leading to localized heating and eventually shorting of the oxide. Kimura [16] used optical measurements which showed that breakdown cross sections are <0.1 m in diameter.

Without deciding exactly how traps are created, it is possible to formulate a statistical model describing oxide wearout leading to breakdown.

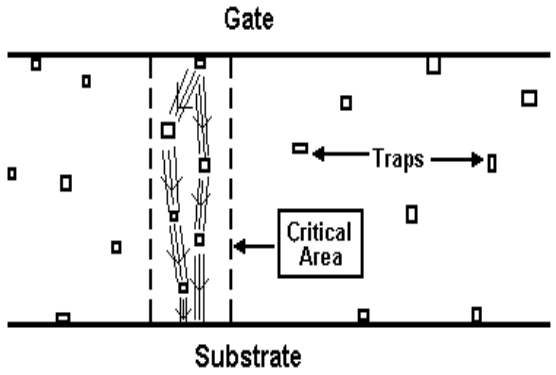


Figure 3 - Defects Leading to High Currents

## Statistical Wearout Model

Dumin's statistical model of wearout [4] is illustrated in Figure 4. In this model, an oxide a given area, LW, and thickness, d, is divided into "N" cells each of area "a". When the number of traps, "n", in a cell exceeds a critical quantity, "nbd", thermal runaway illustrated in Figure 3 occurs. In calculating the failure distribution, traps were assumed to be generated randomly and dispersed throughout the oxide according to a Poisson distribution. The distribution discussed in Figure 1 of this document was created using the Dumin model.

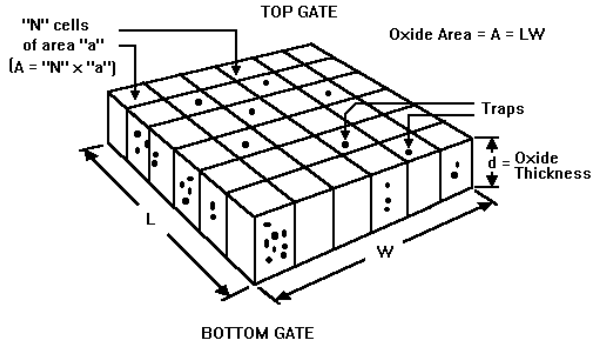


Figure 4 - Statistical Model for Wearout

## Features of Wearout Physical Model

In his 1996 paper, Dumin [15] identified several issues which an oxide wear out model must address and which he maintains his model does. Those issues include:

- trap generation/charging inside tunneling region.
- positive charges near the anode.
- negative charges near the cathode.
- positive and negative charging of the bulk oxide.
- ease in which charge trap states can be changed by subsequent application of low voltage.
- transient flatband voltage shift after stressing.
- presence of interface traps near each interface.
- presence of anomalous positive charge.

## Physical Characterization of Traps

Kimura [16] provides a quantum physical description of wearout concluding that TDDB can be represented by a thermochemical breakdown reaction process. As stated earlier, he also establishes that final shorting of the oxide occurs in a single location. Kimura seems to reach a different conclusion on the source of bond breaking than Dumin [4] or Schlund et al. [14]. However, Kimura's data was taken at very high fields, i.e., 12MV/cm, so his conclusion that degradation is due to generation of hole traps early in the process may be descriptive of a different failure mode than considered by Dumin and Schlund et al.

## Measurement of Trap Generation

Generation of traps under stress is the precursor to final failure according to several papers referenced in this document [4, 5, 7, 10, 11, 12, 15, 18]. In those papers, trap location is not critical. That is, it is not significant whether traps are located at the interface or in the bulk. Trap measurement must include all traps, not just those at interfaces. Thus, techniques which primarily provide interface trap data are not adequate.

Fortunately, trap generation is indicated by charge trapping which is determined by voltage shift at a constant stress current. The number of traps is proportional to dV/dQ for $dQ = I_{DT}$. Figure 5 illustrates how trap generation is derived from a Jramp test with a constant mode. If electron trapping dominates, dV/dQ is positive. It is negative for hole trapping.

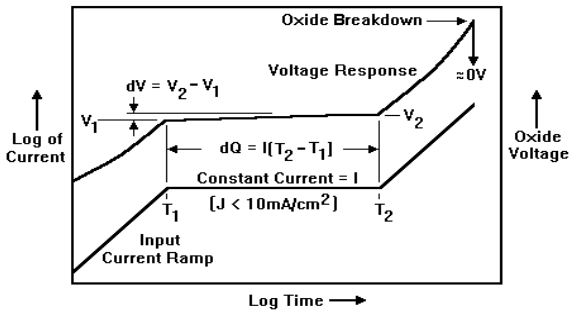


Figure 5 - Voltage Shift at Constant Current

## Detection of Extrinsic Defects

Untested oxides containing defects exhibit much lower than normal voltages when low level current is forced through them. Thus, departure from voltages predicted by tunneling models indicates defects whether caused by thinning, particles, or plasma damage. Klema's paper [17] details testing methods for evaluating oxides at low electric fields.

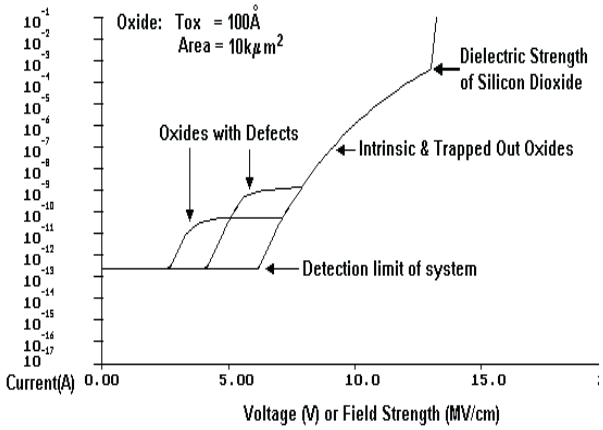


Figure 6 - Defects Leading to High Currents

Figure 6 is a modification of Figure 1 illustrating the appearance of defects on the I-V curve of an oxide. If this test is performed before ramp testing, it is important to keep the maximum voltage well below the "use" voltage specified for the ramp test.

## Ramp Testing Considerations

Gate oxide quality can be assessed using fast ramp techniques at electric fields higher than use levels. Current ramps and voltage ramps produce the same results if care is taken in matching ramp rates and consideration of initial conditions.

Reedholm WLR current and voltage ramps provide constant stress modes which permit trap generation measurements in addition to time to breakdown ($t_{BD}$), charge to breakdown, ($Q_{BD}$), current at breakdown ($I_{BD}$), and voltage breakdown ($V_{BD}$). Such parameters are widely used in evaluating and monitoring oxide quality.

Deciding which parameters to use, and how to use them, is much more of an art than a science. As indicated in the following paragraphs, there are many factors to be considered when evaluating test data.

### Geometric Dependence

Capacitors which are simply flat plates should exhibit higher breakdown parameters than capacitors which emphasize periphery effects from field oxide growth and poly gate etching. Thus, area capacitors should be used as reference devices when evaluating data from periphery capacitors.

### Thickness Dependence of Trap Types

Lisenker [12] plus Apte and Saraswat [11] observe that electron trapping is dominant for thinner oxides while hole trapping dominates at thick oxides. Neither indicate if there is a crossover at which charge trapping cannot be determined from voltage shift at a constant current.

### Quasi-Breakdown

Very thin oxides sometimes exhibit a quasi-breakdown condition which effectively protects the oxide from further damage and minimizes shifts due to a specific stress current. In such cases, careful characterization of the oxide failure mode is needed in order that failure criteria can be set to detect quasi-breakdown when it happens. Otherwise, the ramp test will report anomalous $t_{BD}$, $Q_{BD}$, $I_{BD}$, and $V_{BD}$.

### SILC's and the Time Characteristics of Traps

Early work by Dumin and others reported dc conduction through thin oxides, or stress induced leakage currents (SILC's), as well as 1/t dependence of trap discharging. A recent paper by Scott and Dumin [18] shows that high voltage stress-induced traps do not actually provide means for dc current flow. By using much longer times in assessing trap discharging and charging, they were able to show that oxides with large numbers of stress-induced traps eventually could prevent current flow as well as unstressed oxides. However, they did show that the time constants associated with trap discharging and charging become quite long as trap generation proceeds. For the experiment, they regularly used time delays of 6250 seconds before measuring currents after voltage changes.

Thus, it is quite important to include consideration of measurement times when comparing results on oxides which have undergone voltage stressing.

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