SUPPORT NOTE

SN-107

Test Documentation Requirements

I) Introduction

In order to provide timely and informed technical assistance, Reedholm needs to receive adequate technical information in written or electronic form. Trying to explain what is needed by telephone, or even e-mail, does not convey enough information. Not only do technical requirements need to be stated, diagrams and expected results are needed. All projects that Reedholm contracts to perform must have this level of documentation before technical work is started.

This note illustrates the range and depth of information that is needed to develop a test for a specific test structure—a MOSFET threshold voltage measurement test to be performed on one of Reedholm's fast hot carrier wafer level reliability test structures.

II) The Test Structure

The test structure is a set of three annular transistors in which the drains are enclosed by the gates. The structures share a common source pin, but have separate drain and gate pins. Two of the three transistors share a common substrate pin, while the third transistor has its own substrate pin. Each transistor gate is tied to the bulk by a metal connection to a separate probe pad. This fusible link must be opened before the structure can be measured.

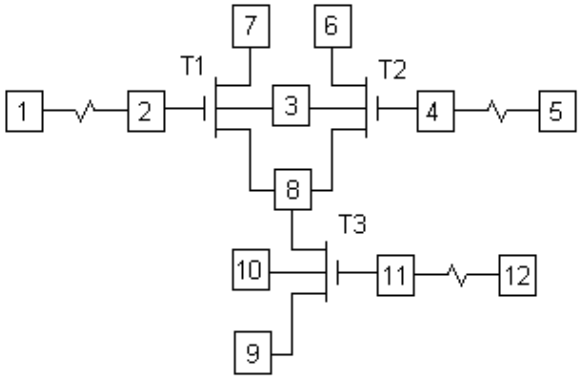

Figure 1 – Multi-Transistor Test Structure

A) Electrical Schematic

Figure 1 is a schematic representation of the test structure. The electrical schematic is important because it shows that the structure is more than simply three separate transistors. That the transistors share a common source, or that two of them share a substrate connection, may prove to be invaluable.

B) Top Layout View

Figure 2 shows the top view of one of the N-channel transistors. Layout is seldom important when transistors perform as expected, but when they do not, the person working on testing can assure him or herself that there is nothing "funny" about the device.

While the transistors shown above would be tested one at a time, there are shared pins and special purpose ones in addition to the single purpose ones. Such complexity is quite normal in test structure design, and usually compromises test results unless properly addressed in setting up tests.

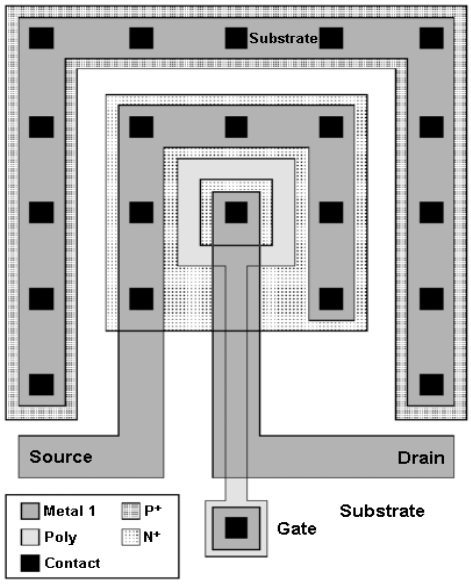

Figure 2 – Annular Transistor Top View

C) Cross Section View

Figure 3 is a view of the HCI N-channel transistor cross-section through the center point of the gate. Just as a top view helps reduce debugging time, so does a cross section—or multiple cross sections.

The top and cross section views do not need to be computer generated. Hand drawn diagrams roughly to scale are adequate for understanding.

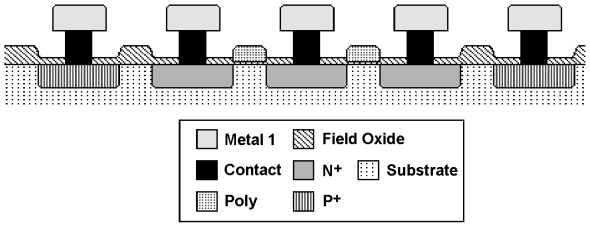

Figure 3 –Transistor Cross Section

D) Structure Identification and Pad Layout

With standardization of probing patterns, it is not always obvious what to test. Wasting time finding the right structure is frustrating, and testing the wrong structure just adds to it. Test structure location(s) and identifying marks are necessary in order to develop or evaluate tests.

For example, Reedholm fast WLR test structures are often located in wafer scribe lines with a label (WLR1) next to pad 1. For one implementation, the 1x12 pad arrays are repeated every fourth row of product die when the wafer notch is facing the probe card edge connector. Pads are 75µm squares placed on 200µm centers and numbered from left to right.

E) Probe Card Connector Assignments

Good test documentation has a map between test pad identification and test system pins. Reedholm developed a software utility to simplify mapping because customers often fail to create this information, or fail to update it correctly. A 3xN table with pad name, pad number, and pin number is adequate.

III) The Test Algorithm

A word description and a simple test schematic is enough for many tests, but ones that are more complex may need a flow chart. In the example for Reedholm hot carrier transistors, the test routine consists of two standard tests for each transistor, one to open the protective fuse, and one to measure the threshold voltage.

A) Opening the Fuse

The first test ramps current into the fuse pin, using a BEM test, with all other pins grounded as shown in Figure 4. Keeping the drain, gate, source, and substrate at the same potential prevents damage to the transistor when the fuse opens. The fuse should open at approximately 90mA (200% resistance increase), at a voltage < 0.5V.

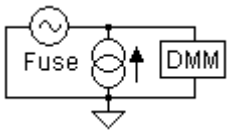

Figure 4 –Fuse Opening Schematic

B) Measuring the Threshold Voltage

Threshold for this application is the gate voltage at a specified drain current when the gate and drain are tied together as shown in Figure 5.

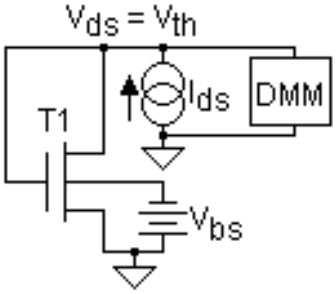

Figure 5 – V_{th} Test Schematic

Pins assignments and threshold measurement conditions are listed in the following two tables.

Size	D	G	S	Sub	Fuse
Minimum	7	2	8	3	2
4X Minimum	6	4	8	3	5
16X Minimum	9	11	8	10	12

Table 1 – Pin Assignments

Parameter	Value
I_{ds}	10µA
V_{ds}, V_{gs} Clamp	2.5V
V_{bs}	Ground
Slew Delay	Enabled

Table 2 – Threshold Voltage Test Conditions

C) Test Considerations

The test structure designer should have identified testing considerations that might compromise test results. In addition, unforeseen testing problems are often encountered once a test structure is used in production. That learning is integrated into good test plan documentation. For example, the following effects might need to be considered when testing transistors.

1) Self-Heating

Because most transistor (bipolar or FET) parameters have high temperature coefficients, test currents cannot be allowed to cause self-heating. Even though it might seem obvious that there is no chance for self-heating, a simple calculation is justified. For the Reedholm hot carrier transistor, these assumptions and calculations assure that no self-heating occurs. Note that if the current below were 1mA, heating would be 2.3C°, or enough to cause a V_{th} shift around 10mV.

- Conduction of silicon ≈ 140W/mC°
- Thermal resistance ≈ 1800C°/W for the smallest transistor. Larger ones with larger areas heat less due to lower thermal resistance.
- Power at 10µA < 13µW, so ΔT ≈ 23.4mC°

2) Charging, Damage, and Light

Properly processed transistors must be able to be turned on and off millions of times in functional circuits without degradation. Therefore, if the test software does not generate voltage spikes beyond the transistor limits, measuring threshold voltage multiple times will not result in parameter changes. However, transistors have significant photoelectric effects, so testing needs to be done with adequate light shielding.

3) Contact Resistance

Currents specified for the Reedholm HCI threshold cause negligible voltage drop even with very high probe contact resistance. However, since blowing fuses requires probe pins with <1Ω contact resistance, testing cannot start with high probe resistance. On a periodic basis, chemical and/or mechanical cleaning, planarity checking, and probe pressure checking must be performed to maintain acceptable probe resistance.

4) Temperature Stability

Since threshold voltage can change one to two millivolts per degree of ambient temperature change, thermal stability in the test area must be maintained and/or considered during correlation.

5) Contributors to Pass/Fail Limits

When determining pass/fail limits, the full range of acceptable process control limits is normally used. However, tighter limits are sometimes used to select wafers that perform better than the process limits imply. Nevertheless, even with the tightest pass/fail limits, instrumentation errors seldom need to be considered. That is because the tightest process span is one to three orders greater than test system specifications.

However, test types based on extrapolation can create large variations in test results. In order to avoid extrapolation errors, a single point measurement was used for the Reedholm HCI test. As a result, possible instrumentation contribution to the allowable errors is insignificant.

IV) Getting the Right Value

Figuring out how to test something, or finding out what is wrong with a test, shouldn't be a guessing game. Some type of device characterization is always needed to be sure that results are correct. For instance, the output characteristics of Figure 6 and the gate characteristics of Figure 7 are adequate for setting up Reedholm N-channel HCI transistor tests.

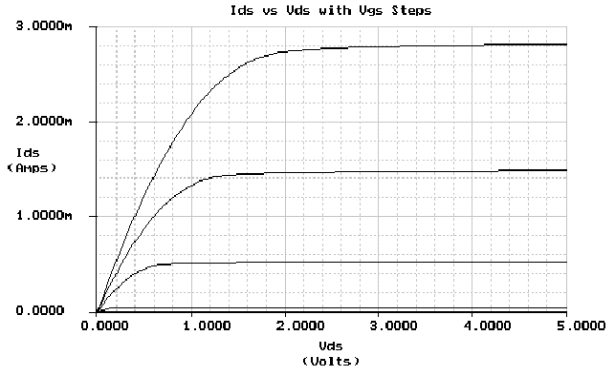

Figure 6 – Output Characteristic Curves

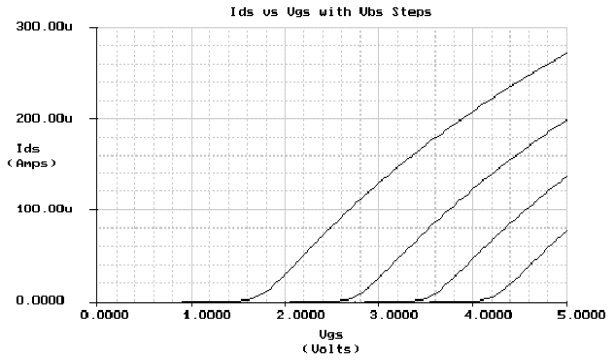

Figure 7 – Transfer Characteristic Curves

V) Proof of Success

After a test is set up, the variability of test results should be evaluated independent of process variations. This information can then be used in setting final pass/fail limits. Reedholm software was developed to simplify gathering statistical information during test plan development.

Figure 8 shows test time and repeatability of the EMPAC test that measured the gate and drain to source voltage required to achieve a drain current of 10μA with a grounded substrate. Notice that the variation is miniscule and that the results are found very quickly. The conclusion is that this test will have no effect on process limits.

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TIMING RESULTS

Elapsed time(sec)  =  719.469m
Test time(sec)     =  7.19469m
Number of loops    = 100
Last result        =  1.65429 Volts
Last result status = Test within limits
Average result     =  1.65433 Volts
Minimum result     =  1.65421 Volts
Maximum result     =  1.6546 Volts
Standard deviation =  54.9574u
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Figure 8 – Timing/Repeatability Analysis

VI) Limitations of "Golden Devices"

While it might seem obvious that use of test structures still on the wafer, or in packages, would be ideal in comparing test systems or test algorithms, that is not the case. Even when a single device is used for comparison, thus eliminating process variations, there are numerous device dependent error sources. These are some of the reasons that semiconductor devices are unsuitable tools for comparing test methods or instruments:

- Photoelectric effects
- Temperature sensitivity (~1%/C° for many transistor parameters)
- Oscillation of high transconductance devices
- Temperature changes from self-heating
- Shifts due to device stress
- ESD with packaged devices
- Test sequence dependence
- Probe contact resistance
- Probe to probe leakage current

Reedholm and other parametric test system vendors provide means of proving compliance with published specifications. Speed, ease of use, and variability of results with speed are reasonable criteria for comparing systems, but accuracy of device parameters is not.