SUPPORT NOTE

SN-127

Test Throughput versus Test Controller Clock Rate

Overview

Despite a 50% difference in clock rates, this note shows there is little difference in test throughput when using 333MHz or 500MHz test controllers.

By inference, running considerably slower or faster controllers would have little effect as long as the clock rate was compatible with the RDS software being run.

Basic Speed Differences

The RI Speed utility software was run to compare times for fundamental routines. For processor dependent routines, times were inversely proportional to controller clock speed. Times in table 1 are in µsec.

RI Speed is one of the tools Reedholm uses to qualify a computer for operation as an RDS test controller.

Procedure	333MHz	500MHz
ReadHdw	2.482	2.300
SendHdw	1.722	1.729
Vrange	8.714	7.564
Arange	38.752	37.509
Volts	17.095	15.132
Volts Measure	60.375	58.687
Sync_Measure	16695.381	16681.764
Amps	19.450	16.188
Amps Measure	64.004	61.696
ConPin	8.283	7.877
DisPin	126.755	120.698
ConDev	4.997	4.093
RI_Delay(1)	1000.106	999.424
MicroDelay40	40.731	42.743
FindRange	2.445	1.625
InstalledUnits	19.082	12.718
0.2 + 16123	0.195	0.130
Ln(1E+20)	1.400	0.926
Sqrt(0.2)	0.588	0.391
Round(0.2)	0.243	0.162

Table 1 - RI Speed Comparison

Testing Times

Three EMPAC tests were compared along with an EMPAC equation. EMPAC is the editor used for test plan generation and maintenance. One of its features is timing of test procedures while gathering statistics on variability of test data. Times below are in msec.

Test Function	333MHz	500MHz
Idss	7.7	7.6
Vt0 PMS	316	315
I@V	7.60	7.46
Equation	0.1356	0.0897

Table 2 - EMPAC Test Times

Probing Simulation

To simulate automatic probing, a test plan with 74 tests was run through ten loops in Acquire. Most customers with DOS based testers store data on servers, so data transfer time for those tests to the network was taken. Network access is not directly comparable because there are many variables including network interfaces, disk speed, memory buffering, etc. Times in table 3 are in seconds.

Transaction	333MHz	500MHz
74 x 10 Tests	307	300
Data Transfer	10	7

Table 3 - Probing Simulation Times

Discussion

Unsurprisingly, timing ratios for procedures and transactions that are clock speed dependent are indirectly proportional to clock ratios. However, ratios for critical timing procedures (e.g., MicroDelay40, RI_Delay, Sync_Measure) are not. Because timing procedures make up the bulk of test code, a 50% difference in clock speed has <3% effect on throughput.

While this was done using RDS DOS, the same insensitivity to clock rates holds for RDS Intranet.