# Overview:
# 0.35µm Test Chip Project

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# Table of Contents Page

## Table of Contents (cont.) Page

# List of Illustrations Page

# Chapter 1

# Company Information

Founded in 1982, Reedholm Instruments, Co., specializes in making automatic test systems. Reedholm's technical knowledge, flexibility, and commitment to forward compatibility have contributed to many advancements in the area of dc test for the semiconductor industry and have led to a world-wide customer base.

## Instrumentation and Fixturing

Instrumentation of Reedholm systems that connects to device test fixtures, such as probe cards and load boards, uses a cross point switching matrix. Even more significant than instrumentation specifications, test fixtures are an integral part of dc semiconductor test systems. In fact, test fixtures represent the limiting factors in accuracy and sensitivity of automatic test systems. To ensure that trustworthy data is gathered with Reedholm tools, analog cabling, probe cards, and load boards are developed and/or characterized specifically for use with these test systems.

## Test System Solutions

With an installed base of over 400 test systems, the scope of Reedholm test services and solutions do not stop with test systems. In fact, test structure design, analysis, and characterization are all aspects of these testing products. Moreover, Reedholm's entire product line is aimed at various aspects of testing structures in one of five categories:

- DC Parametric Systems
- Fast Wafer Level Reliability (WLR) Systems
- Customized Fast WLR Structures
- Packaged Level Reliability (PLR) Systems
- Test Systems for CHARM ® Wafers

For years, parametric testers have performed adequately. However, the semiconductor materials being measured can limit sensitivity, which can result in ineffective data. For this reason, Reedholm concentrates on developing and providing applications software and continual improvement of existing test structures. Instead of perpetual instrument development and characterization, Reedholm develops new instruments only when required for new applications. And to avoid planned obsolescence, Reedholm provides upwards compatibility with new instruments so that test plans written years ago integrate and are adaptable with the latest product offerings.

# Chapter 2

## Wafer Level Reliability (WLR) Programs

WLR, as defined here, involves high acceleration reliability assessment testing on specialized test structures at the wafer level. Stress times are optimized to provide rapid data collection while failure characteristics similar to those achieved using low acceleration levels are produced. Testing is intended for production monitoring on automated probe stations where the typical test time for a given structure is under two minutes. The objective of these wafer level tests is not to generate a quantitative prediction of field reliability but to provide a qualitative indicator of process reliability. This makes the structures and test methods well suited for process control monitoring in the same manner that parametric testing is currently used in production lines. WLR is, therefore, the in-line or end-of-line analog to parametric data collection.

Semiconductor customers' feedback requirements of reliability data cannot be met solely with traditional, long term packaged device testing. Initial process qualification verifies process reliability but cannot ensure that process output will be consistently reliable. In fact, guaranteeing this reliability over time requires verification on a lot-to-lot basis. This can only be done by measuring beyond the traditional zero hour point using accelerated testing techniques.[1] Exact field reliability lifetimes do not need to be extrapolated. Instead, a test is required which is sensitive to the process issues which impact reliability and indicate a change in the baseline qualification reliability levels. Successes with this approach have been numerous.[2,3,4]

Since implementation and sophistication levels of WLR programs vary widely between companies, WLR test data is not available to foundry customers on a regular basis. In fact, WLR has been restricted to localized successes without widespread improvement in how the data is used. For these reasons, the first global demonstration of WLR test structure and methodology effectiveness is currently taking place. This paper describes this approach being taken to encourage the use of WLR and to standardize both structure design and test features.

# Chapter 3

# Profile of the 0.35µm FSA Project

The FSA commissioned a project in order to fabricate, test, and report on a single common set of WLR structures. Reedholm was selected as the supplier for this FSA 0.35µm standard wafer level reliability test chip project. In 1997, Reedholm was awarded the contract to manage the implementation of this project that is targeted at forming guidelines for the standardized use of WLR throughout the industry.

## Origin of the Project

In 1995, the Fabless Semiconductor Association (FSA) chartered a WLR committee to "Champion use of WLR as a standard measure of process reliability in our industry, companies, and foundries. To accomplish this, the committee will:

- Identify standardized test structures and test methodologies and correlate their usefulness.
- Publish data.
- Establish incentives for global adoption of these WLR practices."[5]

Currently, this charter is in progress. Continuing to stimulate interest, the project has grown from the initial six to ten of the world's largest foundries.

## Motivation

The benefits of a WLR program for use as part of larger Building In Reliability (BIR) programs,[6,7,8] burn-in reduction, or process qualifications have frequently been touted. However, these benefits have only been realized within large semiconductor companies[9] that possess the funding to invest in this type of program. However, even within larger corporations, success at one company is not easily replicated at another due to the process specific nature of structures and methods. This has been an inhibitor to WLR proliferation throughout the industry, especially within the fabless-foundry community.

Another factor retarding WLR growth is the logistical complications within foundry relationships. WLR structures, test methods, and expectations vary with each foundry customer. These differences often lead to variation in probe, test, and design elements within a given process. With such disparity between data collected within a given production line, obtaining meaningful information on overall foundry process output and customer acceptance of foundry defined WLR test methods is difficult.

By funding and spearheading a common effort, the FSA is a key enabler of the improvement of acceptance in WLR. A unique feature of this activity is that it includes a significant cross section of foundry customers as well as foundry suppliers. This allows suppliers and customers to work together to mutually define the basis for ultimate WLR program implementation.

As the WLR project progresses, those involved with this effort aspire toward several accomplishments:

- To enable fabless, foundry, and fab companies to benefit from WLR program use.
- To facilitate implementation of a proven WLR program with a common suite of structures.
- To minimize the cost of validating WLR techniques through shared efforts of multiple foundries.
- Allow better comparisons and data sharing through the use of common structures.
- Simplify implementation of WLR test requirements within a fab or foundry operation.
- Proliferate use of WLR as a standard measure of ongoing process reliability.
- Satisfy foundry supplier and customer requirements with a co-developed activity.

# Chapter 4

## Project Method

This project represents a sound approach to WLR standardization. As such, it follows a methodical procedure to ensure acceptance of design concepts and engineering based decisions on overall WLR effectiveness. This includes attention to seven key aspects:

- Structure definition
- Participation
- Prioritization of failure mechanisms
- Structure customization
- Wafer fabrication
- Wafer testing
- Evaluation of the results

The ultimate goal of the project is to mature WLR as a technology, thus enabling it to migrate from a development activity into a production data collection operation.

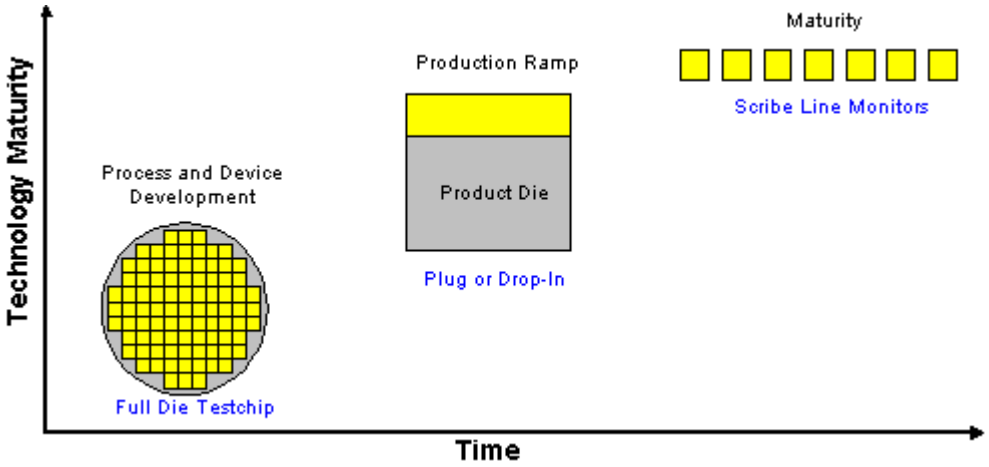



***Figure 1 - WLR Developmental Road Map within a Given Process*** [*]

### Structure Definition

Structure standardization requires both clear definition and documentation of test structure design concepts and of test methodologies. These aspects are being accomplished by using a combination of WLR test experience, literature searches, and split lot experiment results. Another factor of structure definition involves defining the ultimate aims for the WLR structures. The structures are eventually intended for use within scribe lanes. Limited size and dimensions of the structures allows their use only for intrinsic failure monitoring rather than for extrinsic (or defect) failure detection with large area devices. Documentation of these structure design features, formulas, layouts, and test methodologies is compiled and defined.

[*] Figure 1 is courtesy of Test Chip Technologies.

## Participation

Although initial participation funding included six selected commercial foundries, awareness of the project has grown through the fabless community, and additional foundries continue to join by funding their own participation costs. As of August 1998, ten foundries are in active participation. To ensure buy-in of participating foundries, a thorough design review was held to communicate the documented elements of each WLR structure. This involved technologists from each foundry as well as fabless representatives. All of these individuals indicated satisfaction with the structure design objectives and capabilities.

## Prioritization of Failure Mechanisms

Predominant process failure mechanisms have been prioritized to focus first on the mechanisms of most interest to the industry and to process technologists. For example, a process utilizing chemo mechanical polishing techniques for inter-level planarization would not require a structure to monitor step coverage or spin-on-glass (SOG) charging. A listing of the failure mechanisms in order of importance is provided in Table 1. Discussion of these mechanisms follows this project summary.

| Failure Mechanism (in Ranked Order) | Measured Parameters |
|---|---|
| Fast Hot Carriers (N & P Substrates) | $\Delta V_t$, $\Delta Gm$, $\Delta I_{leakage}$, $\Delta I_{saturation}$ |
| Gate Oxide Integrity (Area & Edge Intensive) | $Q_{bd}$, $V_{final}$, $I_{final}$, Test fail conditions, $I_{leakage\ (pre,\ post\ ramp)}$, $I/V_{const\ stress}$ |
| Process Induced Damage | $\Delta V_t$, $\Delta Gm$, $\Delta I_{leakage}$, $\Delta I_{saturation}$ |
| Metal Electromigration | $t_{fail}$, $T_{stress}$, $J_{stress}$, $AF_{measured}$, $R_{initial}$, $R_{last}$, $I_{stress}$ |
| Gate Oxide Charge Trapping (N & P Substrates) | $\Delta V_t$, $\Delta Gm$, $\Delta I_{leakage}$, $\Delta I_{saturation}$ |
| Via Electromigration | $t_{fail}$, $T_{stress}$, $J_{stress}$, $AF_{measured}$, $R_{initial}$, $R_{last}$, $I_{stress}$ |
| Via Voiding | $I_{heater}$, $V_{heater}$, $T_{heater}$, $R_{thermometer}$, $t_{stress}$ |
| Mobile Ion Contamination | $\Delta V_t$, $I_{heater}$, $V_{heater}$, $T_{stress}$, $R_{thermometer}$, $t_{stress}$ |
| Junction Spiking | $I_{heater}$, $V_{heater}$, $T_{heater}$, $R_{thermometer}$, $I_{leakage(init,\ max,\ last)}$, $t_{stress}$ |
| Contact Electromigration | $J_{stress}$, $T_{stress}$, $AF_{measured}$, $R_{last}$, $t_{stress}$, $R_{initial}$, $R_{reference}$, $I_{stress}$, $t_{fail}$ |
| Interlevel Dielectric Strength | $V_{bd}$ |
| Metal Stress Migration | $t_{fail}$, $T_{stress}$, $J_{stress}$, $AF_{measured}$, $R_{initial}$, $R_{last}$, $I_{stress}$ |
| Top Passivation Strength | $Q_{bd}$, $V_{last}$, $R_{max}$, $R_{last}$, $R_{initial}$, $R_{reference}$, $T_{rise}$, $t_{ramp}$, $I_{final}$ |
| Spin-On-Glass Charging | $\Delta V_t$, $I_{heater}$, $V_{heater}$, $T_{stress}$, $R_{thermometer}$, $t_{stress}$ |
| Metal Step Coverage | $t_{fail}$, $T_{stress}$, $J_{stress}$, $AF_{measured}$, $R_{initial}$, $R_{last}$, $I_{stress}$ |

***Table 1 - Sample Data Parameters***

## Structure Customization

The process technology targeted for this project is a 0.35µm CMOS logic process. This geometry and technology was chosen based on the qualification and production status within the foundry community at the time the project began. When chosen, the 0.35µm process geometry was desirable because it had been used in production and had an established qualification baseline. This selection criterion was used to ensure that new failure mechanisms or process issues did not create confusing WLR test results.

While each participating foundry has virtually identical design rules, test structures require some customization on a per-foundry basis. Regardless of process physical dimensions, layer electrical differences require structure layout variations to provide the same levels of acceleration

for a given mechanism. For example, a salicided poly process with a 4Ω/☐ sheet resistance requires a narrow poly heater to remain with test system compliance limits, while a non-salicided poly process with a 40Ω/☐ sheet resistance requires a wider heater. Both structures deliver similar heating characteristics for failure acceleration. However, each structure is specified to provide particular levels of acceleration (temperature, current, voltage, electric field, etc.) with layouts customized to achieve the specified stress acceleration targets.

## Wafer Fabrication

WLR test chips, like the one shown in Figure 2, are fabricated on three lots at each foundry. One normal lot and two experimental lots are fabricated to provide sufficient test sites for meaningful WLR evaluation. A minimum of seven wafers from each fabricated lot are sent for testing at a central test facility. This eliminates any contribution of test hardware or software differences to the test results.

The large task of validating WLR techniques through designed experimentation has been distributed among project participants. Although highly competitive in the marketplace, each company recognizes the benefit it would receive through participating in this project and in sharing information. Therefore, each participant has been assigned one of the 15 failure mechanisms listed in Table 1. Foundry technologists are designing experiments to aggravate the assigned mechanism.

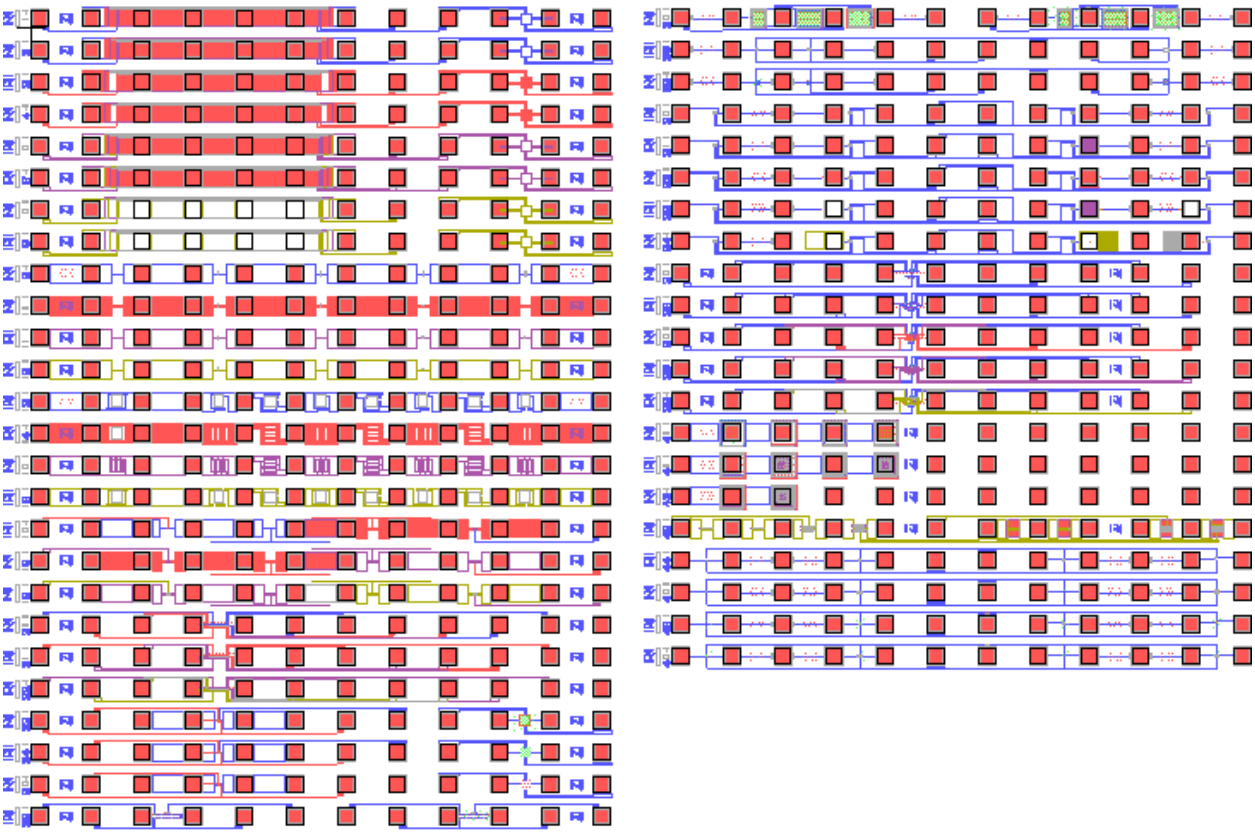


***Figure 2 - WLR Test Chip (1-Poly, 4-Metal CMOS)***

## Wafer Testing

The evaluation of WLR structures' effectiveness is data intensive, with 1500+ test parameters measured for each test chip. Examining five sites per wafer, seven wafers per lot, three lots per foundry, all from ten foundries, over 1.7 million data points are being measured and summarized.

## Evaluation of the Test Results

One guiding aspect influencing WLR validation focuses on assuring that data from WLR monitoring does not differ from normal process variation found wafer-to-wafer or lot-to-lot. Otherwise, only overly severe process shifts would be detectable. This aspect of WLR validation is accomplished through the analysis of WLR results across the known good lots, across wafers within the lots, and across multiple fabrication locations. Data is reported to demonstrate structure stability with normal process variations and its suitability as a statistical process control tool.

At the same time, WLR structures must be sensitive enough to detect potential reliability degradation due to process deviations. This is accomplished through designed experiments for each of the failure mechanisms targeted for these WLR structures. In conjunction with the structure stability information demonstrated from the normal lots, these experiments indicate the ability of WLR structures to detect process reliability shifts and their effectiveness as a process monitor.

# Chapter 5

# WLR Test Structures

The WLR test chip has 138 individual testable structures in 47 total 1x12 pad arrays (Figure 2). While this is too large of a test suite both in size and test time for production use on every lot, it includes structures for the dominant process reliability failure mechanisms. An early objective of any WLR effort is to determine the subset of WLR structures, test methods, and output parameters that are of primary concern for a given process. Below some of the design or test features are elaborated upon.

## Hot Carrier Injection

Rapid testing for hot carriers has presented a challenge for reliability testing. Conventional stress methods that bias the transistor to achieve peak substrate current cannot be accelerated beyond their existing levels without causing device junction breakdown. Other methods attempt to simulate channel hot carriers through avalanche breakdown of the drain-substrate diode. However, any hot carriers generated in this method are too far from the channel area and the gate oxide to cause hot carrier damage to the gate area.

To balance the need for rapid results and for valid acceleration of the hot carrier mechanism, the stress method being used incorporates a source/substrate bias with the drain and gate at ground potential with a current meter on the gate. The stress bias voltage is pre-characterized to remain well below the Fowler-Nordheim tunneling current level for the device. Doing this eliminates the tunneling current conduction mechanism from contributing to gate current. This stress method produces significant gate current that cannot be contributed to leakage or to tunneling currents and generates large transistor characteristic shifts even with $I_G$<1nA.

## Gate Oxide Integrity

The designated test structure and methodology comply with the EIA/JEDEC EIA/JESD35-1 and EIA/JESD35 design specifications.[10,11] Six capacitors are included in the gate oxide pad set: three NMOS and three PMOS. Each polarity includes an area intensive, a ploy edge intensive, and a field edge intensive capacitor. All three oxide structures for each polarity have the same drawn oxide area, which allows for better comparisons of $Q_{BD}$ or similar values.

A common mistake made in the design of test capacitors for highly accelerated testing is to make multiple connections to the capacitor top plate so that voltage drop across the capacitor area may be minimized. While these connections will reduce the magnitude of the voltage drop, they cannot eliminate it altogether due to the fact that current is tunneled through the capacitor during testing. Unfortunately, when this type of over connection is made to capacitors, it includes additional field oxide edges within the capacitor design. This can leave the area and poly capacitors susceptible to failures attributed to field edge mechanisms. Reedholm's design provides for minimal contacts to the capacitor top plate and minimizes the amount of "parasitic" field oxide edges on the area and poly edge structures.

While antenna ratios for the structures are not large, process induced charge damage is possible from the charge collected on the gate pad connection. To prevent process charge damage from

occurring, the capacitor top plates are shorted to the substrate at metal 1. These fuses are opened prior to device testing.

The test method provides unique insight into the trapping of the oxide during the ramped breakdown test. By measuring the voltage required to maintain a constant current through the capacitor area, the presence and amount of trap generation or filling can be monitored (Figure 3). An output plot of the current ramp test showing current as a function of time illustrates this stress method. An increase in voltage over the constant current segment indicates the filling of traps while a decrease in this voltage indicates the generation of oxide traps.

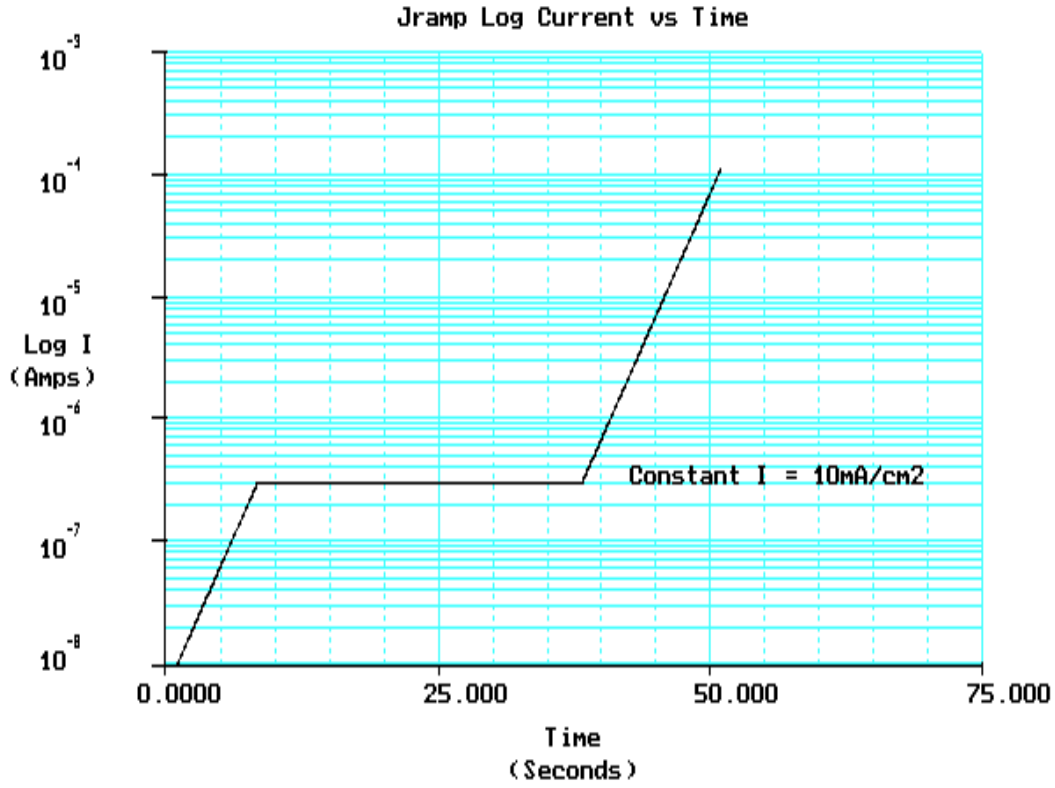



***Figure 3 - Current Ramp Characteristics***

## Process Induced Damage (PID)

Due to the numerous sources of process damage (ion implant, deposition, etch, ash, and clean) at each layer of semiconductor fabrication, many monitors are needed to verify that none of the sources will cause a reliability problem. Multiple, minimal geometry transistors have gate electrodes connected to antennas of different material and characteristics with a pad size area[12] (Figure 4). Each conductive layer has three antenna designs—plate, mesh, and contact/via arrays—that sensitize the structures to the different charge damage sources within the process.

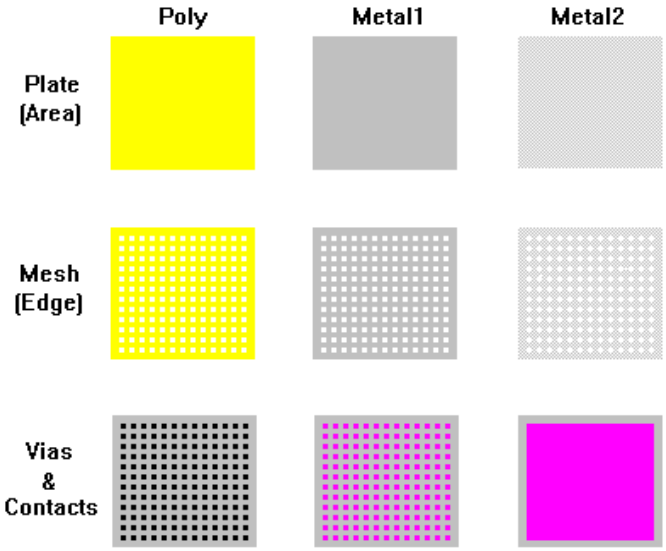



*Figure 4 - Antenna Arrays for 1-Poly, 2-Metal Process*

To limit the device sensitivity to only the targeted layer, fuse connections short the gate electrode to the substrate on the next metal deposition step (Figure 5). This fuse is opened prior to transistor characterization (Figure 6). In conjunction with the antenna devices, a reference device is tested to enable a report of the net transistor parameter shift from the reference. This allows normal process variation to be eliminated from the reported results and to increase the overall test structure sensitivity.

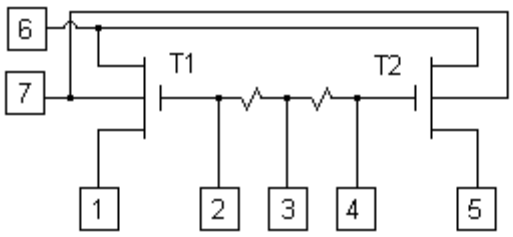



*Figure 5 - PID Structure Schematic*

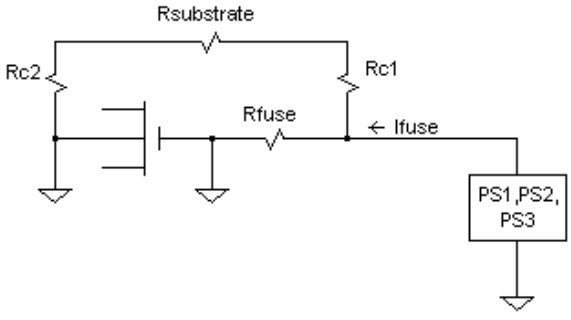



*Figure 6 - Protection Fuse Blowing Schematic*

## Metal Electromigration

Past attempts at metal electromigration focused on the Standard Wafer-level Electromigration Acceleration Test (SWEAT) structure, which has known problems in terms of complexity and physical correlation to line electromigration.[13] A review of the physics behind the electromigration mechanism resulted in Reedholm developing a much different structure for highly accelerated WLR testing (Figure 7).

Two structures are designed for each metal layer using 800µm lines of both minimum and 3µm widths. The design provides the necessary temperature uniformity across the structure in two ways: the length of the structure provides a uniform thermal profile across the effective test area due to the test structure length;[14] the test area is also surrounded on all sides with conductive layers to thermally "bottle" the test line and to prevent adjacent pads or features from affecting the thermal profile. These design considerations provide for accurate temperature feedback as well as good stress control with $T_{PEAK}/T_{AVG}$=1.04, much better than with a SWEAT approach.

A van der Pauw resistor within the test area provides a mechanism for reducing the effects of normal process line width variation on the test results. This has been shown to significantly improve the data spread and the extrapolation for highly accelerated electromigration testing.[15] Finally, the structure includes elements for lower acceleration testing with Babel tower current source and sink connections and with extrusion monitors.

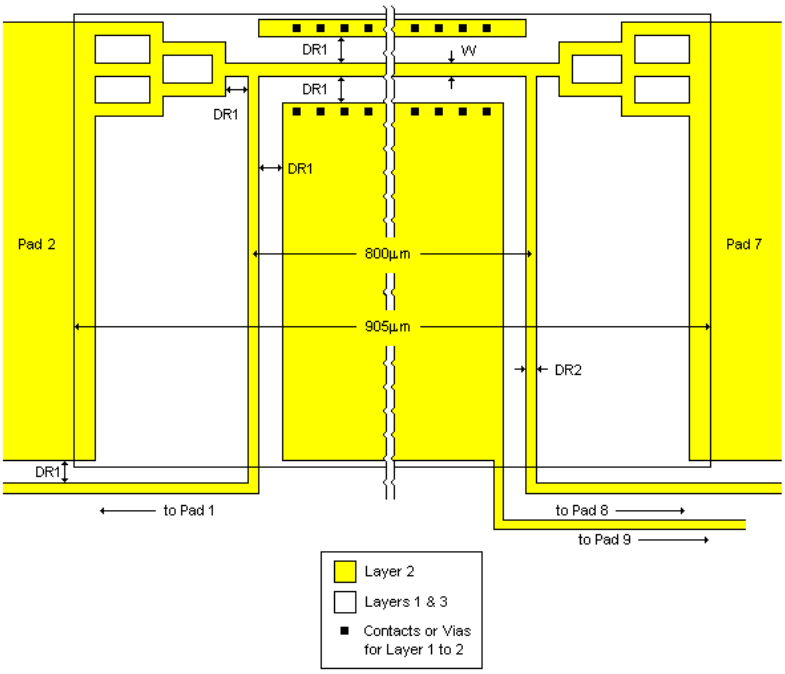



***Figure 7 - Metal Electromigration Structure***

## Gate Charge Trapping

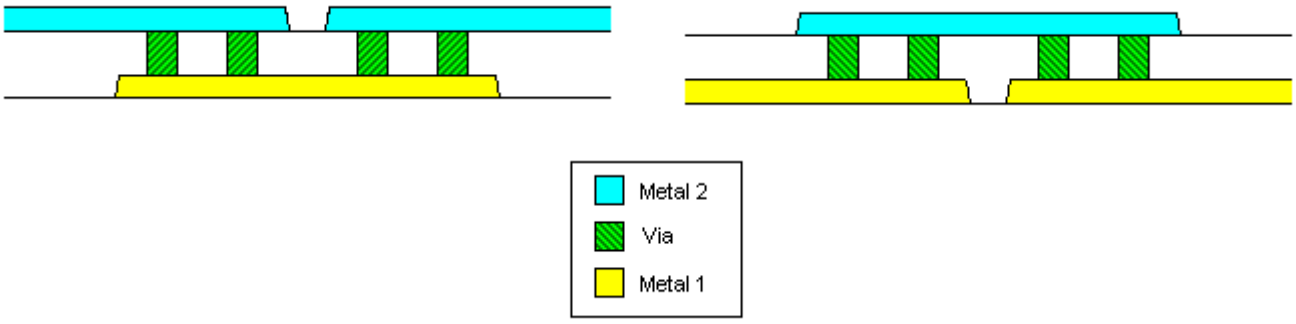
Gate trapped charge detection requires a large area gate device to increase the probability of trap occurrence within the tested device. The device under test must also be protected from process induced charge damage. Even for large area devices, significant antenna ratios exist for test transistors since the gate pad acts like a 100+:1 charge collection antenna. This PID protection is done by fusing the gate to the substrate at metal one and later opening the fuse to make the device testable.

Most trapped charge damage can be annealed by subsequent processing but later come back to affect the reliability of the device. A test sequence that will reveal such damaged sites is required. This test sequence consists of first opening the protection fuse to allow full characterization of the test transistor. Next, transistor parameters are measured and stored before applying a low level tunneling current stress. Then, transistor parameters are re-measured and shifts are calculated.

## Via Electromigration

Single via chains have been found to be inadequate for highly accelerated stress testing due to the large amount of localized heating at the via-metal interface for tungsten plug technologies. This localized heating is caused by a combination of the current density increase at the plug and the tungsten's high resistivity as compared to the metal alloy. Also, standard via chain structures do not provide the ability to determine which side of the via failed.

The test structure design addresses these issues in two ways. First, a calculated number of vias are arranged in parallel to minimize localized heating around the vias. The appropriate number of vias depends upon the via and metallization resistivity values. Second, two via chains are designed to evaluate the upper and lower via interfaces separately. The first structure evaluates the lower via-metal interface (Figure 8a), since the upper metal link is shorter than the Blech length, and will inhibit electromigration in that layer.[16] The second structure (Figure 8b) works similarly except for the upper via-metal interface.




**(a) Upper Via-Metal Interface** **(b) Lower Via-Metal Interface**

***Figure 8 — Via Electromigration Structure***

The structure failing location should be at the cathode end via array due to the preferential migration of aluminum in the direction of the current flow. To electrically verify the failure location after testing, a sensing tap connects to the center via chain link to allow resistance measurements of both via arrays. Also included are two reference structures that match the geometry of the upper and lower metal layers used. Time-to-failure for the via chain and reference structures can be compared to eliminate the contribution of metallization reliability factors from the via-metal interface reliability testing.

## Via Voiding

Voids, caused by air gaps or contaminants within vias, can propagate with time and can eventually lead to via failure. Since this mechanism is accelerated by thermal cycling of the via chain, a polysilicon or buried layer heating element is used for this WLR testing. The structure consists of a via chain, two reference lines (one that is used as a thermometer) from the same metal layers used in the via chain, and a polysilicon heater (Figure 9).

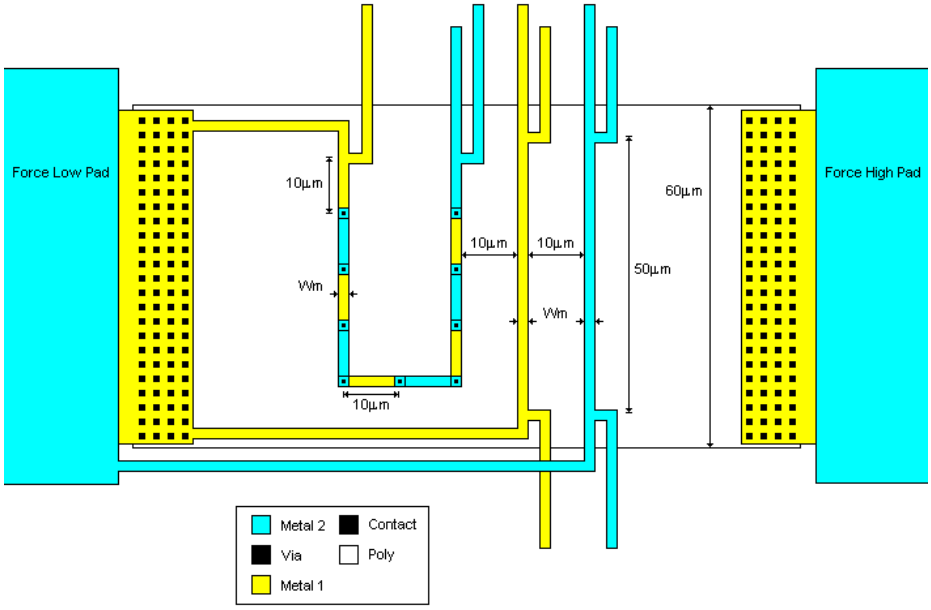



***Figure 9 - Via Voiding Structure***
***(From left: Via Chain, Metal 1 and Metal 2 Thermometer / Reference)***

The test method involves monitoring the via chain and reference line resistance values before and after several thermal cycles. Since the polysilicon heater can heat and cool in milliseconds, many cycles with very large temperature variations can be performed in a short time. The reference lines contain the same amount of each metal layer used in the via chain. Any resistance change caused in the reference metal layers is a result of metal stress void growth, not via void growth. The reference structure resistances can then be subtracted from the via chain to show the net resistance change contribution of the vias. This allows accurate monitoring of small changes in via resistances for the structure and ensures that only the via-metal interfaces are monitored during testing.

## Mobile Ions

Mobile ionic contamination is measured using a field transistor at each poly and metal layer. A polysilicon heater enables temperatures up to 500°C to be delivered to the oxide area and provides for heating of the test area in milliseconds rather than the minutes required with a hot chuck. With thermal excitation of the mobile ions, a poly or metal gate provides biasing to move ions toward the Si-$SiO_2$ or $SiO_2$-Gate interface. Threshold voltages of the field transistors are monitored before and after the biased thermal cycles. A thermometer meandering over the heater area completes the structure to provide accurate temperature monitoring (Figure 10).

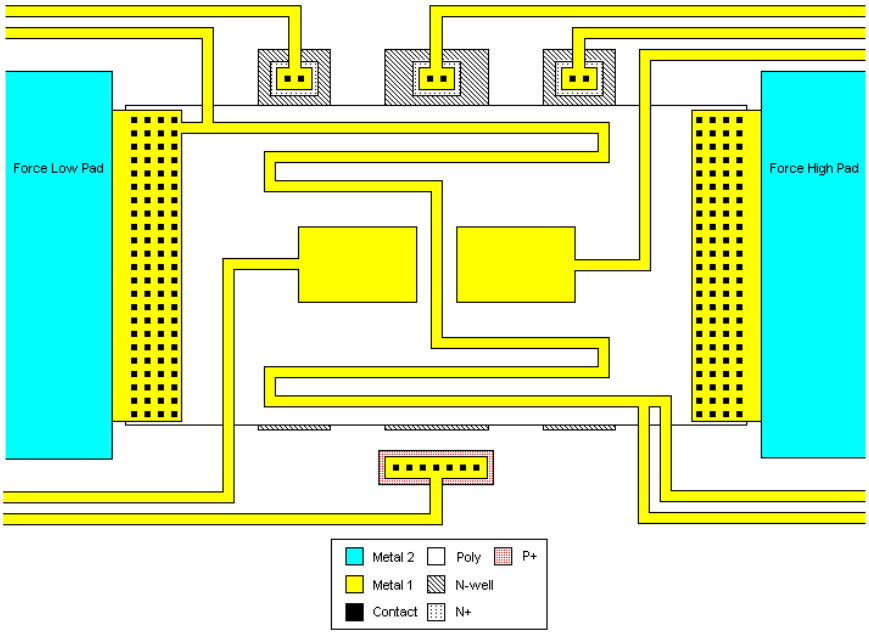



***Figure 10 - Mobile Ion Structure***

## Stress Migration

Stress migration remains of significant importance to semiconductor processing, and structures are designed for highly accelerated testing for this mechanism. However, there is questionable payback for the space and time allocated for such structures. This is primarily due to the related failure mechanism physics. Stress migration is heavily time dependent. Propagating tensile stresses due to thermal mismatch between oxides and conductors into voids can take weeks. However, if voids do occur and are present at the end-of-line testing where these WLR structures would be monitored, the test structure will highlight them.

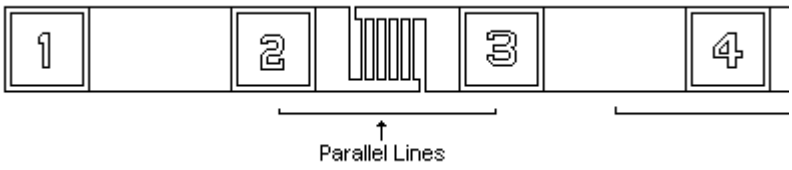



***Figure 11 - Stress Migration Reference Structure***

To detect the presence of voids, the test compares time-to-failure values from a reference and monitor structures for a given metal layer. The reference structure contains multiple identical segments in parallel to minimize the impact from a void that could be present within the reference area (Figure 12). This simple arrangement shunts current around a potential void laden reference segment. The monitor consists of identical size test segments arranged in series with alternating X and Y orientations (Figure 12). This prevents the structure from having wafer placement sensitivity due to any radial stresses.

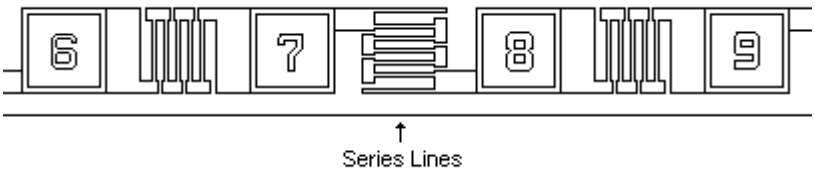



***Figure 12 - Stress Migration Monitor Structure***

Techniques utilizing a ramped breakdown method cause catastrophic failure and prevent effective analysis of the failure location. To address this undesirable result, a time-to-failure method can be more effective in detecting line voids. This approach also allows stress to be halted before full opening of the test line in order to preserve the void and allow failure analysis.

# Chapter 6

## Summary

The advantages of a well developed, mature WLR program have been touted through the years, but these benefits have not been easily replicated. The efforts of individual foundries to use these designed experiments to demonstrate structure effectiveness and statistical data will assist in verifying WLR's value as a process monitor. Thus, the FSA project proliferates the use of Reedholm WLR structures and test methods for semiconductor process that is significantly advancing WLR as a technology.

# Chapter 7

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