RDS 2.0 PARAMETRIC TEST SOFTWARE

- **IE Replaced By Windows Application**
- **Test Plan Generator**
- **Built-in Curve Tracer/I-V Sweeps**
- **MSSQL Database**
- **GPIB Prober Drivers**
- **System Maint. (Calibration, Self Test)**
- **DR YIELD SW for Plots, Maps, Reports**

Overview

Reedholm's test executive software is designed for automated semiconductor parametric testing. It provides a complete solution, along with an easy to use UI. All test routines are built in, so code development is not necessary, but is available. Everything is stored (test plans, conditions, results) in a single database hosted on a current, networked, fully supported version of SQL server.

This data driven software environment makes programming optional. Many find the use of standardized test types leads to better data and faster test times, resulting in more actionable data with as much as 3.9x more throughput compared to other legacy systems.

The file based formats of the 1980's eventually became the RDS Intranet versions of the new century. The offering was expanded to include an SQL database and simplification of the editing process from the original "Q&A" test plan creation process to one of filling in cells for a given test type.

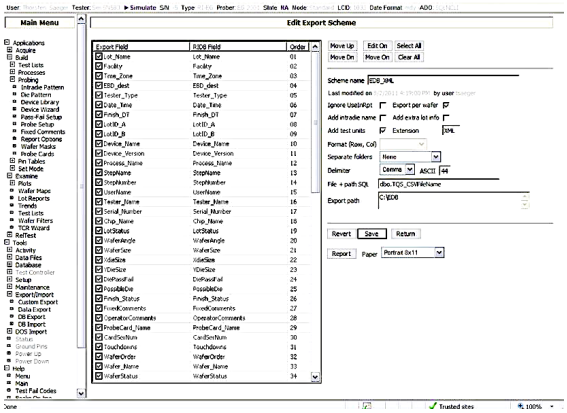


Figure 1 - Database Export Scheme

RDS 2.0 Deliverables

This release continues the evolution of the data driven software environments, while providing a thoroughly modern approach to parametric testingthat can be fully supported by today's IT departments and device/test engineers.

The Internet Explorer (IE) interface from RDS Intranet is eliminated and the obsolete elements have been replaced. It is a natural upgrade path for customers of the legacy Reedholm systems, as well as a starting point for new customers that want to leverage off a platform proven to be suitable for high volume test operations.

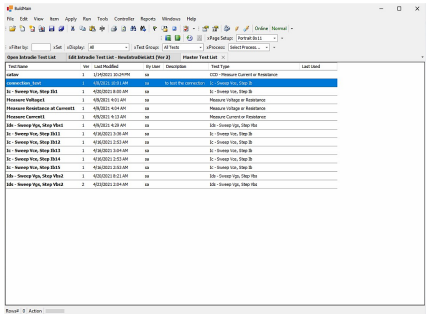


Figure 2 – Intradie Test List

Customers running either the classic RDS-DOS software versions (8.1 or later) and/or RDS Intranet software should be able to update to RDS 2.0, Deliverables include:

- Reedholm SW version 2.0
- DR YIELD SW for graphical display of trend charts, wafer maps, I-V plots and the like.
- Engineering services (Migration, training).

Test Plan Hierarchy

The test plan elements required to do automatic testing involve more than just test lists and probing patterns. These elements include processes,devices, pin tables, reports, pass-fail criteria, and prober control options. The following diagram illustrates the test plan hierarchy:

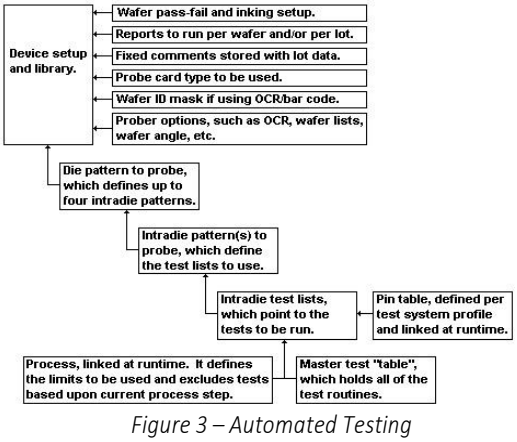


Figure 3 – Automated Testing

Test Plan Creation

RDS 2.0 contains a comprehensive set of test routines that cover bipolar, depletion FET, and enhancement FET technologies implemented on Si, GaAs, GaN, and SiC materials. Years of experience supporting customers resulted in a robust, fast, and flexible test engine with these features:

- Prober driver and probe site editor.
- Lot reports and test data exporting.
- Version control of test library and plans.
- Test routine code documentation.
- Test conditions (pins, voltages, etc.).
- System manuals and training guides.

With RDS 2.0, one can program every routine from scratch, or leverage off the library of field proven test routines that have tested millions upon millions of devices:

2 Terminal Resistance – Force Current or Voltage
3 Terminal Voltage or Resistance
4 Terminal Voltage, Resistance, or van der Pauw
Beta at an Ib, Ic or Ie
Calculate Delta Length
Current at a Voltage
Early Effect
gm or Vt at an Ids or % of Ids
gm or Vt at 2 Ids, 2Vgs, or PMS
High Voltage (+2kV) Continuous & Snapback BV
Ic – Sweep Vce, Step Ib
Ic – Sweep Vce, Step Vbe
Ic and Ib – Sweep Vbe
Ids – Sweep Vds, Step Vgs and Vbs
Ids – Sweep Vgs, Step Vbs
Ids – Sweep Vgs, Step Vds
Ids at a Vgs
Isub – Sweep Vgs, Step Vds
Measure Capacitance at 0V, ±100V, or +2kV
Measure Capacitance – Sweep ±100V or +2kV
Measure Current or Voltage
Measure Current – Sweep Time
Measure Current – Sweep Voltage
Measure Current at High Voltage (+2kV)
Measure Resistance – Low Bias
Measure Resistance – Sweep Voltage
Measure Resistance at Current
Measure Resistance (4T) – Sweep Current
Measure Resistance at Voltage
Measure Voltage – Low Bias
Measure Voltage – Sweep Time
Measure Voltage (4T) – Sweep Current
Peak Beta
Replace Test Parameters with Prior Results
Saturated Vt
Small Signal Beta
Standalone Equations & SQL Extractions
Step Voltage Until Current
Stress at a Vgs
Stress Current
User Written Test
Vgs at an Ids, % of Ids, or Peak Isub
Voltage at a Current (±100V or +200V)

Figure 4 – Available Test Types

Dozens of fields in a database record are populated when setting up a test. That record is downloaded to a test controller and executed in real-time without any delays for compiling. Setting up and controlling test plans is similar to populating spreadsheet files. The test engine supports:

- Multiple pins per DUT leg (drain, gate, etc.).
- Biasing and grounding extra DUT pins.
- Forcing voltage or current on extra pins.
- Executing user input equations.
- Using prior test results for test conditions.

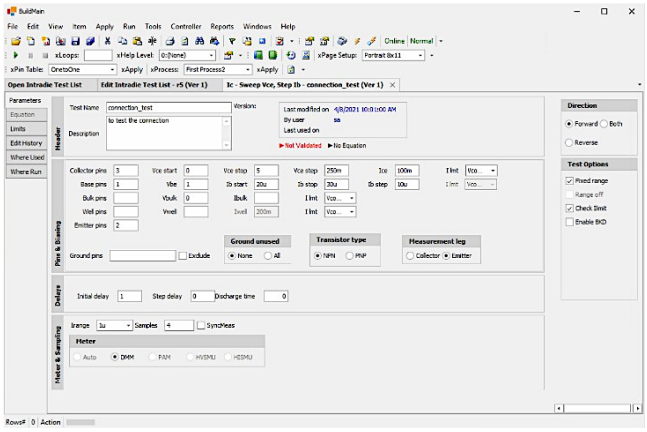


Figure 5 – Build Input Page

After a test is created and found effective, being in record format makes it easy to copy and use as the starting point in setting up a new test.

Setting Up Test Plans with BUILD

The test list edit screen lists the tests set up to be run in production. New and existing tests can be inserted, cut, copied, etc. Tests to be skipped upon test passing or failing can also be set.

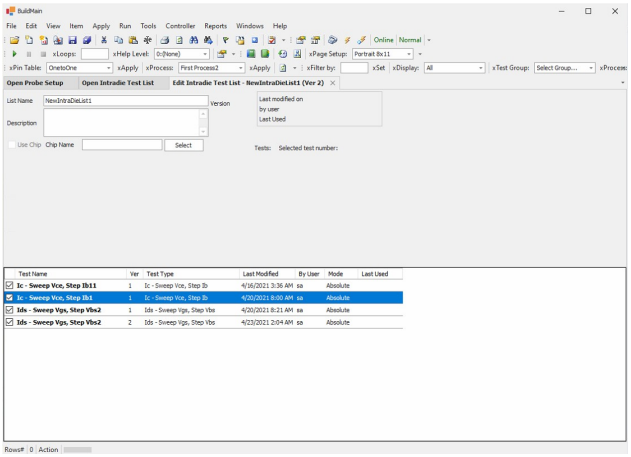


Figure 6 – Build Intradie List

Tests can be executed within Build to look for interaction issues between tests/structures. If the checkbox next to test is filled, that test will be executed during automatic probing. This allows for including characterization tests in a test list that could come in handy when troubleshooting.

Setting up Die Patterns

The graphical die pattern editor is used to quickly create probe patterns, including the 9 site pattern oneshown in figure 7.

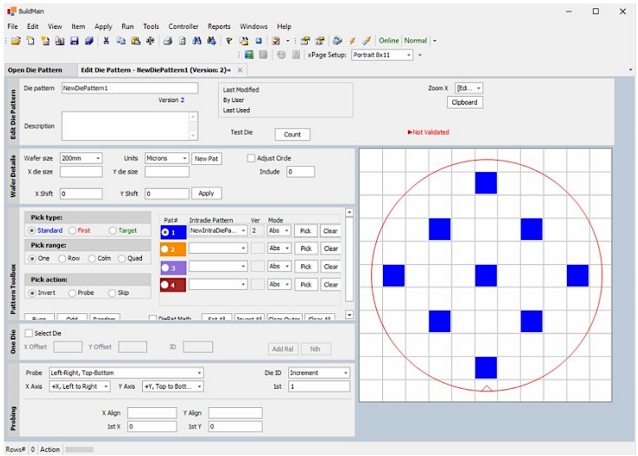


Figure 7 – Die Editor

Other die pattern editor features include:

- Up to four different test patterns can be run.
- Separate die move and prober alignment sizes.
- Single die X & Y offset step for misplaced PCMs.
- Separate target and first die locations.
- Tool to select all die and remove outliers.

Sub-moves are called Intra-Die moves in the application and are shown below:

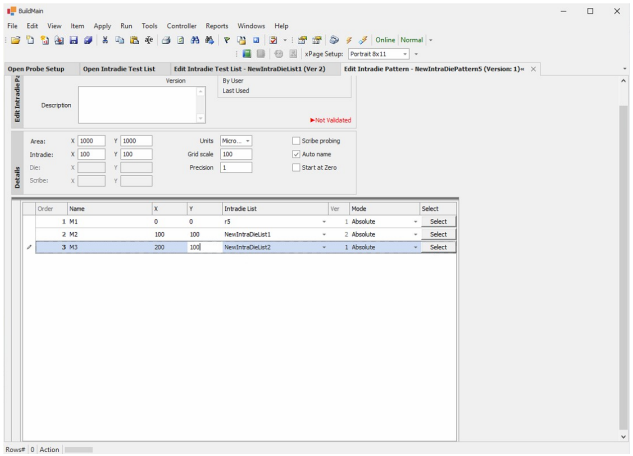


Figure 8 – Set up Prober

Quality Data AND Fast Test Times

RDS 2.0 allows the system to take data like a curve tracer inclusive of the prober analog cable. Thus, it is no longer necessary to take a wafer to another station to generate characteristic curves and then try to match results between systems.

This capability can eliminate uncertainty about device behavior and what test conditions to use to assure the highest quality data. A curve, or set of curves, can be created for nearly every test type.

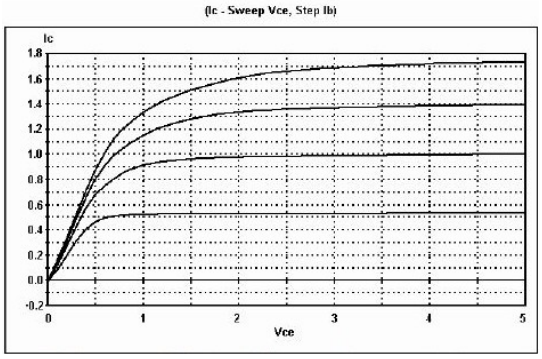


Figure 9 – IV Data

Prober Control

GPIB or IEEE-488 drivers exist for most commercial probers, and new ones can be developed. Some of the selections used for settingup the prober are shown below:

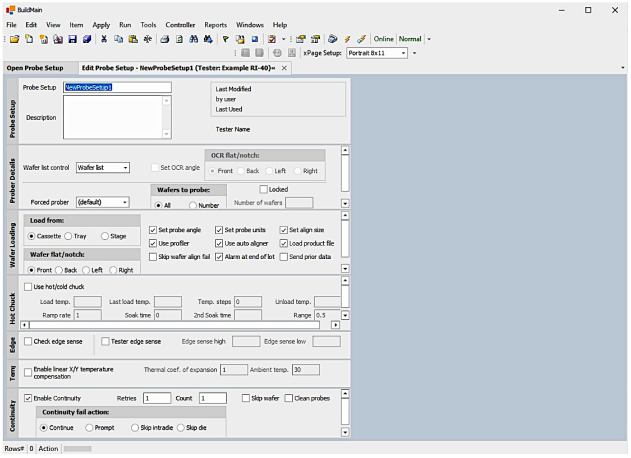


Figure 10 – Prober Setup

Maintenance Tools

Software tools ensure that thesoftware, computer hardware, and instruments are running within specification, to calibrate the modulesif necessary, and to troubleshoot and identify failing modules.

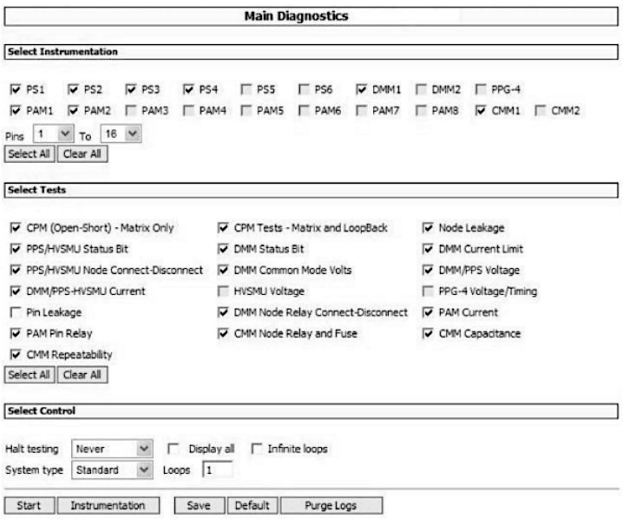


Figure 11 – Diag. Setup

SQL Database

The Reedholm database is named RIWEBSQL. Tables in this database serve many purposes. The UI tables hold the text labels, screen information, text messages, and data-binding properties for all of the screens and menus. There are temporary tables (whose names begin with "tmp_ and zimp_") that serve as a kind of 'scratch paper' for stored procedures, including storing raw data for imports and exports.

The test plans and device designs are organized in still other tables, which support multiple versions and locking of records to keep production processes secure. There are also the various test data tables, where lot data, plot data, and reliability data are saved for future extraction and analysis. Finally, numerous tables exist to manage the database and were created and are maintained by MS SQL Server software. Most of these tables start with "sys".

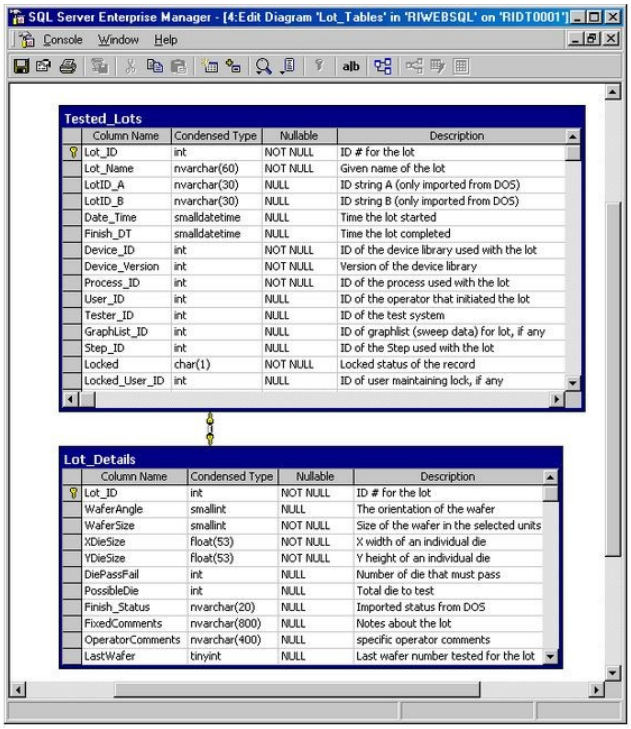


Figure 12 – UI Table

Validating Everything Works

Before a lot can be started, the data entered and their associated elements such as probing patterns, test lists, etc., must all be validated—which occurs when the Validate button is clicked. The validation involves hundreds of checks to ensure proper operation/validation including:

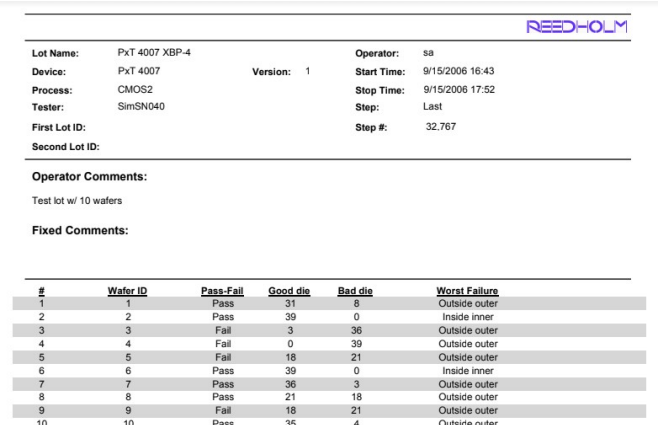
- Making sure all tests have limit tables for the selected process.
- That the probing patterns are correct.
- That the elements that make up a device (probe setup, pass-fail setup, reports, etc.) are all working correctly.
- That none of the items to be used are currently being edited.
- That the device must be released.
- That the probe/DUT card touchdown count has not exceeded the maximum.

Once all the test parameters have been validated, the test sequence for the lot can be started. Starting a lot also results in the application controls and menus being disabled, preventing errant interruptions from halting lot testing. Once the lot has finished testing and unloading the last wafer if applicable, controls and menus are enabled again.

Reports

Reports are generated through third party DR YIELD applications which pull data directly from the storedtest results that can also be accessed from the database. Reports include:

- Raw data using engineering notation w/4digits.
- Lot summary for all wafers, engineering notation w/4 digits and showing target value.
- Wafer pass-fail summary by test.
- Wafer pass-fail summary by die with # die to pass.
- Wafer pass-fail summary by die with % die tofail set at 45%.
- Wafer process time summary.
- Execution time summary of each test in lot.
- Limits, target, units, and order of tests run inlot.


REEDHOLM

Lot Name:	PxT 4007 XBP-4			**Operator:**	sa
Device:	PxT 4007	**Version:**	1	**Start Time:**	9/15/2006 16:43
Process:	CMOS2			**Stop Time:**	9/15/2006 17:52
Tester:	SimSN040			**Step:**	Last
First Lot ID:				**Step #:**	32.767
Second Lot ID:					

Operator Comments:

Test lot w/ 10 wafers

Fixed Comments:

#	Wafer ID	Pass-Fail	Good die	Bad die	Worst Failure
1	1	Pass	31	8	Outside outer
2	2	Pass	39	0	Inside inner
3	3	Fail	3	36	Outside outer
4	4	Fail	0	39	Outside outer
5	5	Fail	18	21	Outside outer
6	6	Pass	39	0	Inside inner
7	7	Pass	36	3	Outside outer
8	8	Pass	21	18	Outside outer
9	9	Fail	18	21	Outside outer

Figure 13 – Wafer Die Test Results