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1.2kV Class SiC MOSFETs with Improved Performance over Wide Operating Temperature

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***Abstract*—In this paper, we report on 1.2kV SiC MOSFETs rated to $T_{j,max}$=200°C, exhibiting improved performance characteristics across operating temperature. Our devices show stable, rugged and reliable operation when subjected to industry standard qualification tests. Low on-resistance of 35mOhm/79mOhm at T_j=25°C and 47mOhm/103mOhms at T_j=150°C are shown for 0.1cm² and 0.2cm² die. 1000 hour High-Temperature Gate-Bias (HTGB) tests at T_j=200°C show excellent threshold stability with less than 5% parametric shift observed. High-Temperature Reverse Bias (HTRB) at T_j=200°C/V_{DS}=960V also show stable and reliable operation. Single-pulse avalanche energies of over E_{Av}=1.75J are obtained with 0.1cm² MOSFETs.**

I. Introduction

Advances in material quality and availability, device development and fabrication process maturity has pushed SiC MOSFETs to the brink of insertion in a range of power electronics applications such as renewables/solar, transportation and aviation industries where size and weight reduction, increased functionality and reduced bill-of-materials cost are becoming realizable. While SiC MOSFET entitled performance benefits versus incumbent IGBTs have been widely reported in the 1.2k-1.7kV voltage class, acceptance has been limited due to increased die cost and limited reliability data presented to date. In this paper, we present reliable, T_j=200°C rated SiC MOSFETs while offering low on-resistance with minimal chip size.

II. Approach

To address SiC MOSFET acceptance barriers, our development approach is to fully capitalize on their potential benefits by:

- Design for high-temperature reliability and operation
- Minimize die size and maximize $I_{DS,Max}$
- Employ simple, high yielding fabrication processes

The increased functionality offered by 1.2kV (and above) SiC MOSFETs have made them attractive to power-density sensitive early adopters despite their higher early (low-volume) component costs [1]. However, these military and aerospace applications often require well-defined qualification and de-rating guidelines. In reference [2], NASA specifies that maximum operating temperature should be 20% lower than the maximum rated temperature. For example, a device with $T_{j,max}$=150°C could be operated only up to 120°C in such applications. This limits operating currents below the datasheet values, and requires more SiC area to meet application needs.

Additionally, SiC MOSFETs should be designed to minimize losses across a range useful operating conditions while maximizing the conduction efficiency of the SiC chip. Typical benchmarking such as specific on-resistance $R_{On,sp}$ versus blocking voltage (at T_j=25°C) are used to illustrate the entitlement of early technology demonstrators. However, they offer limited information to actual users and can be misleading when considering practical constraints such as current rating, switching loss, die scaling limitations etc. Fig. 1 shows the results of this work comparing normalized SiC die area at more typical operating conditions of T_j=150°C.

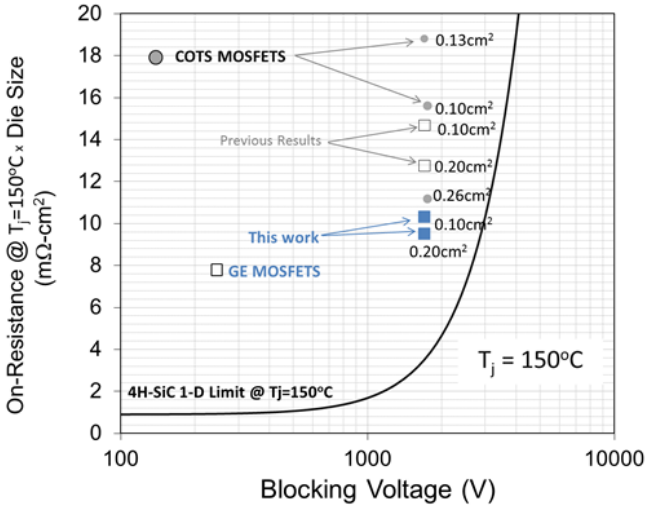

Figure 1. On-resistance at T_j=150°C normalized to SiC die size from various MOSFET suppliers [3]-[6]. Tj,max=150°C is specified for commercially available (COTS) devices.

Our low on-resistance across operating temperature allows us to achieve low conduction losses with minimal die size. By offering high-temperature SiC MOSFETs with low losses and minimal overhead, we can minimize the SiC material cost contribution in volume production and offer more advantageous balance-of-system tradeoff with simplified cooling systems.

III. Results and Discussion

In this section we present the industry's first T_j=200°C rated SiC MOSFETs as evidenced by our 1000 hour High Temperature Gate Bias (HTGB) and High Temperature Reverse Bias (HTRB) results on 2.25x4.5mm (20A, nominally) devices, N=77. These reliability assessments were performed in accordance with AEC-Q101 qualification standards [7]. We also illustrate the performance of our 1.2kV MOSFETs with low on-resistance and excellent ruggedness.

A. Demonstration of $T_{j,max}$=200°C SiC MOSFETs

High Temperature Gate Bias (HTGB)

Threshold instability has been a reported issue in commercially available SiC MOSFETs in the past, but has improved such that latest available components have seen their $T_{j,max}$ increased to 150°C [3],[5]. However, this remains below the maximum junction temperature of the incumbent 1.2kV Si IGBTs. In Fig. 2, we show HTGB results from a 1000 hour stress of T_j=200°C, V_{GS}=23V ($V_{GS,Max}$). There were no device failures logged from the MOSFET samples run. To our knowledge, these are the first SiC MOSFETs reported to demonstrate parametric stability under these conditions [7].

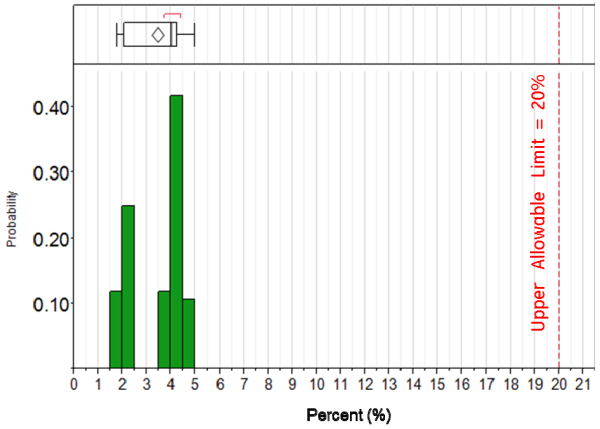

Figure 2. Percent change in VGSTH (10mA) threshold voltage distribution after 1000hr/T_j=200°C/V_{GS}=23V/HTGB stress, 2.25x4.5mm SiC MOSFETs from 3 wafers packaged in TO-247s

Parametric comparison of device characteristics measured after 1000hrs/200°C/V_{GS}=23V HTGB exhibited less than 5%, threshold voltage drift, which is safely below the 20% maximum required by the target qualification standard [7]. All other device characteristics also exhibited acceptably small differences, such as on-resistance ΔR_{On} < 1.2% and 1.2kV drain leakage current $\Delta I_{DSS1200V}$ < 2x, safely below the specification limit of 5x. These results indicate that our SiC MOSFETs exhibit acceptably low Positive Bias Threshold Instability (PBTI) at the maximum gate-drive voltage and T_j=200°C, providing safe margin for users.

Large Negative Bias Threshold Instability (NBTI) has also been observed in early generation SiC MOSFETs [8]. This threshold instability can occur in the presence of negative Gate-Source bias at high-temperatures. Despite the normally-off operation of these devices, users commonly apply a negative gate bias in the off-state to improve switching performance and add noise margin. Fig. 3 shows the measured threshold voltage of our SiC MOSFETs versus stress time when subjected to T_j=200°C, V_{GS}=-15V. The measured parameters remained stable after our 165hour evaluation, with a measured threshold voltage shift of ΔV_T<1.3%.

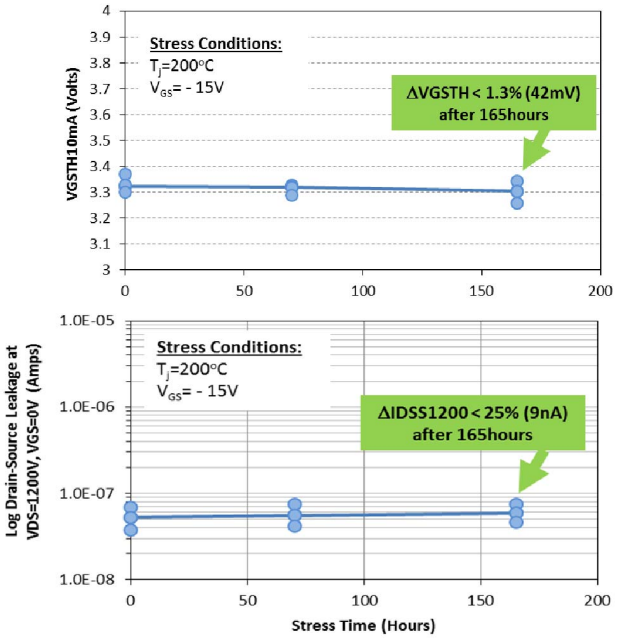

Figure 3. VGSTH (10mA) threshold voltage and IDSS1200 Drain-Source leakage current (V_{GS}=0V, V_{DS}=1200V) versus stress time at V_{GS}=-15V, T_j=200°C, 2.25x4.5mm SiC MOSFETs packaged in TO-247s

High Temperature Reverse Bias (HTRB)

A batch of SiC MOSFETs (2.25mm x 4.5mm) from the same lot and wafers were subjected to HTRB stress for 1000hours at T_j=200°C and V_{DS}=960V (80% of rated voltage) per [7] and no device failures were logged. All devices tested showed excellent parametric stability with a maximum threshold voltage change of $\Delta V_{GSTH,Max}$=6%, maximum $\Delta R_{On,Max}$=1.5%, and drain leakage current $\Delta I_{DSS1200,Max}$ =18%. Fig. 4 shows the drain leakage current distribution of the sample population before and after 1000hour/T_j=200°C/V_{DS}=960V HTRB stress. The distribution remained well below our datasheet upper specification limit USL=10µA, with a post-HTRB median leakage of approximately 34nA.

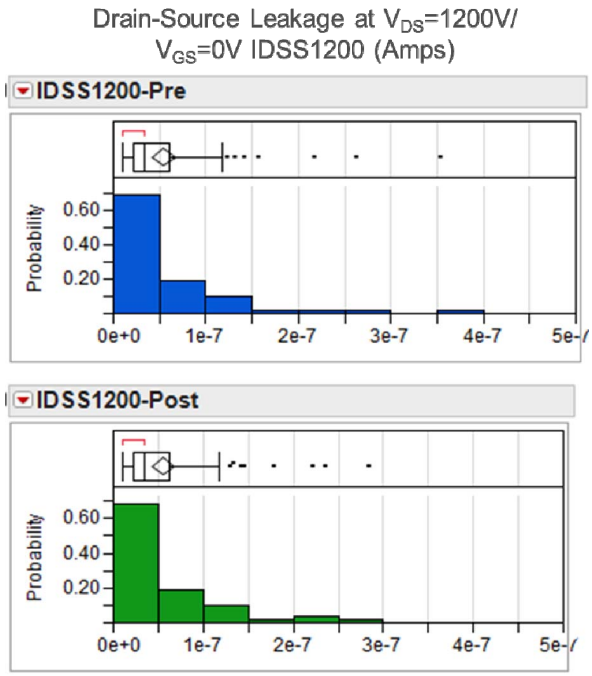

Figure 4. IDSS1200 Drain-Source leakage current at V_{GS}=0V, V_{DS}=1200V before (Pre) and after (Post) 1000hr/T_j=200°C/V_{DS}=960V/HTRB stress, 2.25x4.5mm SiC MOSFETs from 3 wafers packaged in TO-247s

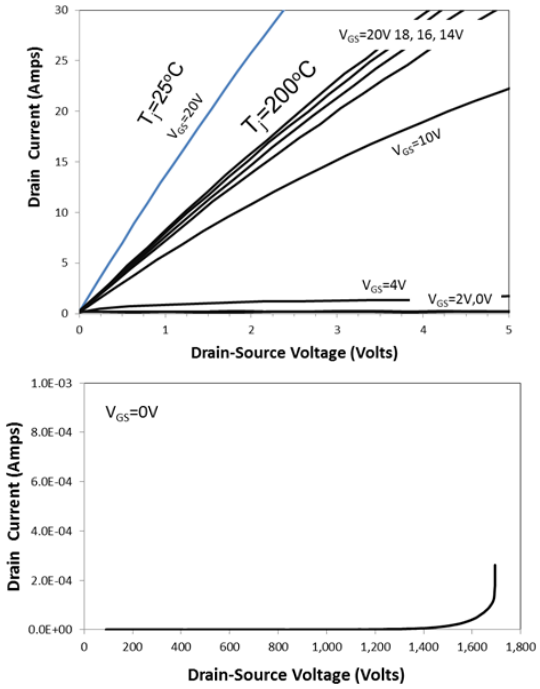

Figure 5. Drain family I-V characteristics of 0.1cm^2 SiC MOSFETs (2.25x4.5mm) packaged in TO-247

The results presented in this section show the ability to rate our SiC MOSFETs to $T_{j,MAX}$=200°C. Thus, even under typical 20% de-rating guidelines [2], users can better exploit the benefits of SiC and safely design for junction temperatures that are beyond those of existing Si IGBTs [9].

B. Performance versus Temperature

Following from the design approach described in the preceding sections, we have also improved the on-resistance of our SiC MOSFETs across a wide range of useful temperatures. In this section, we present the characteristics of our 0.1cm^2 (2.25x4.5mm) and 0.2cm^2 (4.5x4.5mm) SiC MOSFETs. Fig. 5 shows a typical drain family output characteristics of a typical 0.1cm^2 device. The on-resistance (taken at I_{DS}=20A/V_{GS}=20V) is 79mOhms at room temperature and increases by roughly 35% to 103mOhms at T_j=150°C. At $T_{j,Max}$=200°C, the device offers a low on-resistance of 130mOhms, respectively (see Fig. 6). The on-resistance of these devices are roughly 30% lower than existing commercial SiC MOSFETs at T_j=150°C, despite having smaller total die area.

Fig. 7 shows the room temperature on-resistance of larger, 0.2cm^2 (4.5x4.5mm) MOSFETs measured at V_{GS}=20V and I_{DS}=45A. The sample shown are devices packaged in TO-247s from a single wafer. The mean on-resistance is 35mOhm with a small standard deviation of approximately less than 1.5mOhm. The on-resistance increases to 47mOhm at T_j=150°C and to 58mOhm at 200°C.

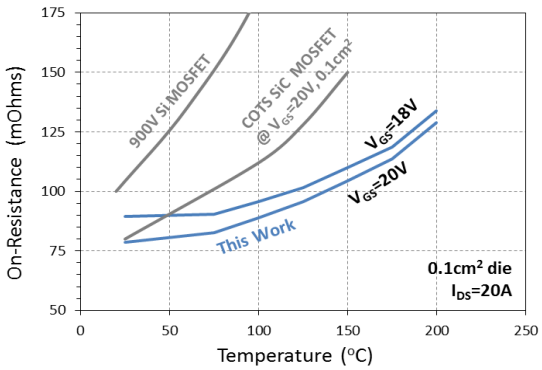

Figure 6. On-resistance of 0.1cm^2 SiC MOSFETs (2.25x4.5mm) packaged in TO-247 versus temperature, I_{DS}=20A, V_{GS}=18V, 20V shown

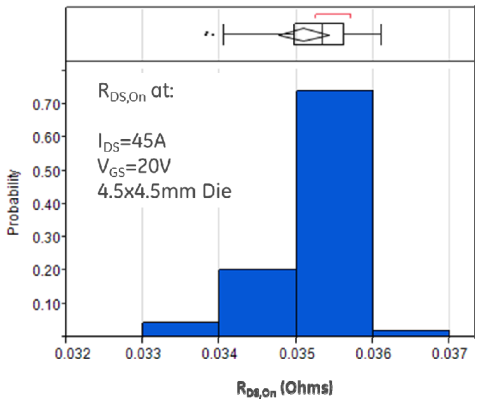

Figure 7. On-resistance of 0.2cm^2 SiC MOSFETs at I_{DS}=45A, V_{GS}=20V, Sample: devices from one wafer packaged in TO-247

C. Avalanche and Short-Circuit Ruggedness

SiC MOSFETs also offer avalanche ruggedness which is desirable in the presence of inductive loads, stacked topologies and large area multi-chip modules. Our SiC MOSFET design exhibits excellent avalanche capability. Un-clamped Inductive Switching (UIS) tests show single-pulse avalanche energies greater E_{Av} > 1.7J for the 0.1cm^2 die (see Fig. 8 showing V_{DS} and I_{DS} waveforms under avalanche). Of six samples tested, four reached the limits of our setup (1.7-1.8J) and could not be failed. None of the larger 0.2cm^2 MOSFETs tested (sample size=6) could be failed with the same setup.

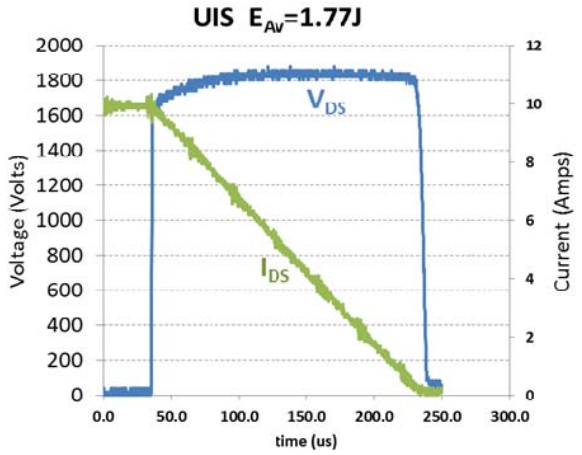

Figure 8. Un-clamped Inductive Switching (UIS) waveform of 0.1cm^2 (2.25x4.5mm) SiC MOSFET

Short-circuit ruggedness is one area where IGBTs typically excel over MOSFETs, offering safe short-circuit times of t_{SC}=10µs or more [9], [10]. We have tested the short-circuit ruggedness of these low resistance 1.2kV SiC MOSFETs as a function of V_{DC}. Fig. 9 shows the short-circuit results from a 0.1cm^2 device measured with V_{DC}=600V and V_{GS}=20V. The peak current is 300A and the measured time-to-fail is t_{SC}=6.8µs, respectively.

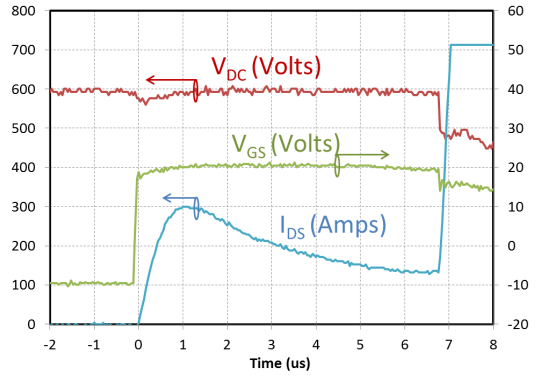

Figure 9. Short-circuit withstand time of 0.1cm^2 (2.25x4.5mm) SiC MOSFETs tested with V_{GS}=20V and V_{DC}=600V

Decreasing V_{DC} voltage to 480V results in t_{SC}>11µs while increasing the voltage to 720V reduced the time-to-failure to t_{SC}=4.5µs. At 960V (80% of rated voltage), the short circuit withstand time was reduced to t_{SC}=3µs. The peak current remained approximately the same for all V_{DC} conditions indicating that the devices retain gate control. The t_{SC} can be improved (to 9µs with V_{DC}=600V) at marginal costs in on-resistance by lowering V_{GS} to 18V. Although not equivalent to Si IGBTs, these t_{SC} results should be adequate for most high-frequency application needs.

IV. Conclusions and Future Work

In this paper, we have presented our progress towards reliable, high-performance, T_j=200°C rated SiC MOSFETs in the 1.2kV voltage class. For the first time, 20A SiC MOSFETs are shown to safely meet survivability and parametric stability requirements when subjected to industry standard qualification tests such as 1000hour/200°C High Temperature Gate Bias (HTGB) run at $V_{GS,Max}$=23V and High Temperature Reverse Bias (HTRB) run at 80% of rated blocking voltage (V_{DS}=960V). We have also demonstrated superior performance with SiC MOSFETs across temperature range spanning from T_j=25°C to T_j=200°C. When compared to latest commercially available SiC MOSFETs, the devices presented here exhibit comparable on-resistance at room temperature but 30% reduction at T_j=150°C. These characteristics allow us to maximize the benefits of SiC MOSFETs by combining superior temperature rating enabled by threshold stability and gate oxide reliability with improved parametric performance over useful temperature range.

Acknowledgment

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